

# SF2

Rev: 1.0

## Page Index =====

### Revision History :

1. Ver A: Initial
2. Ver B:
  - (1) Add North Bridge Fan Sink Header
  - (2) Delete SATA Crystal
  - (3) Modify USB, AUDIO, S/P DIF Out, Front Panel Headers for ACER
  - (4) Add SATA Status LED Signal via Front Panel
  - (5) Modify USB Power Source on South Bridge due to SiS AP note
  - (6) Add One More Fuse for 1394 Header
  - (7) Add SPDIF02 Header (Pitch 2.0mm) for HP S/P DIF Out
  - (8) Modify Hardware Reset Circuit
  - (9) Modify VCCVID Power Good Circuit
  - (10) Remove IR, SIRQ Headers
  - (11) Add JP4, JP5 Headers for HP
  - (12) Modify CPU Fan Control Circuit
  - (13) Change RT9173 for DDR Vtt
  - (14) Change LAN Connector Type
3. Ver 1.0:
  - (1) Add C289, MC40 for EMI Solution

1. Cover Sheet
2. Block Diagram
3. Clock & Power Distribution
4. Socket478-1
5. Socket478-2
6. Decoupling Circuit
7. SiS661FX-1 (HOST / AGP)
8. SiS661FX-2 (Memory)
9. SiS661FX-3 (VGA / HyperZip)
10. SiS661FX-4 (Power)
11. SiS964-1 (PCI / IDE / HyperZip)
12. SiS964-2 (Misc. Signals)
13. SiS964-3 (USB)
14. SiS964-4 (Power)
15. Main Clock
16. Clock Buffer
17. DDR DIMM 1, 2
18. DDR Termination
19. AGP slot
20. VGA / IDE Connectors
21. USB Connector
22. PCI Slot1, 2
23. PCI Slot3
24. LAN
25. IEEE1394
26. Audio Codec
27. Audio Interface
28. Super I/O
29. KB/MS/ROM/FDC/IR
30. COM 1,2 / LPT
31. HM/FAN/RING/LPC
32. Voltage Regulator
33. DUAL 5V, 3V& SB Regulator
34. VRD10 (CPU Vcore)
35. ATX / Panel / RTC
36. BOM and GPIO Attention



**SIGNATURE**


**DATE**

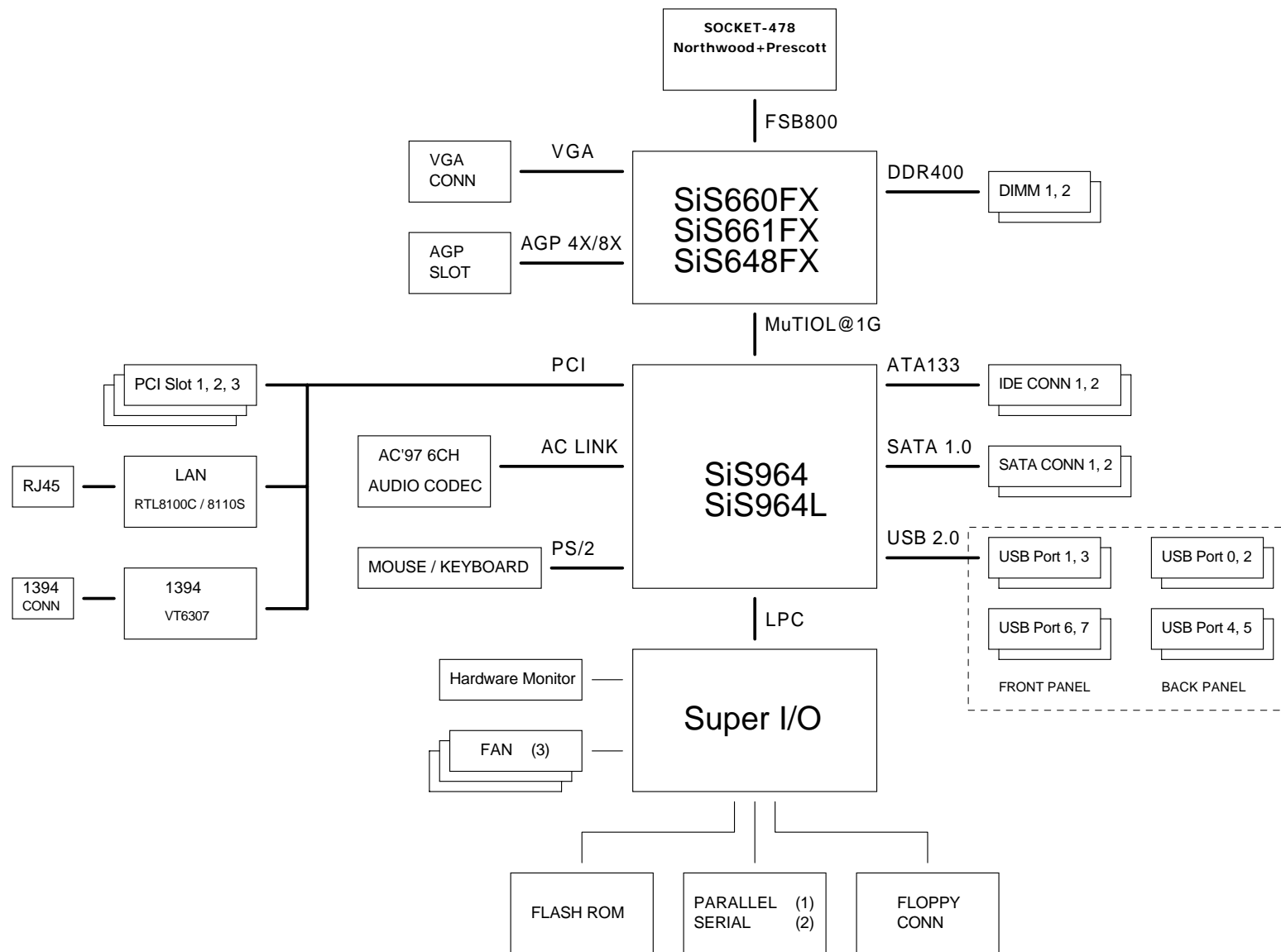
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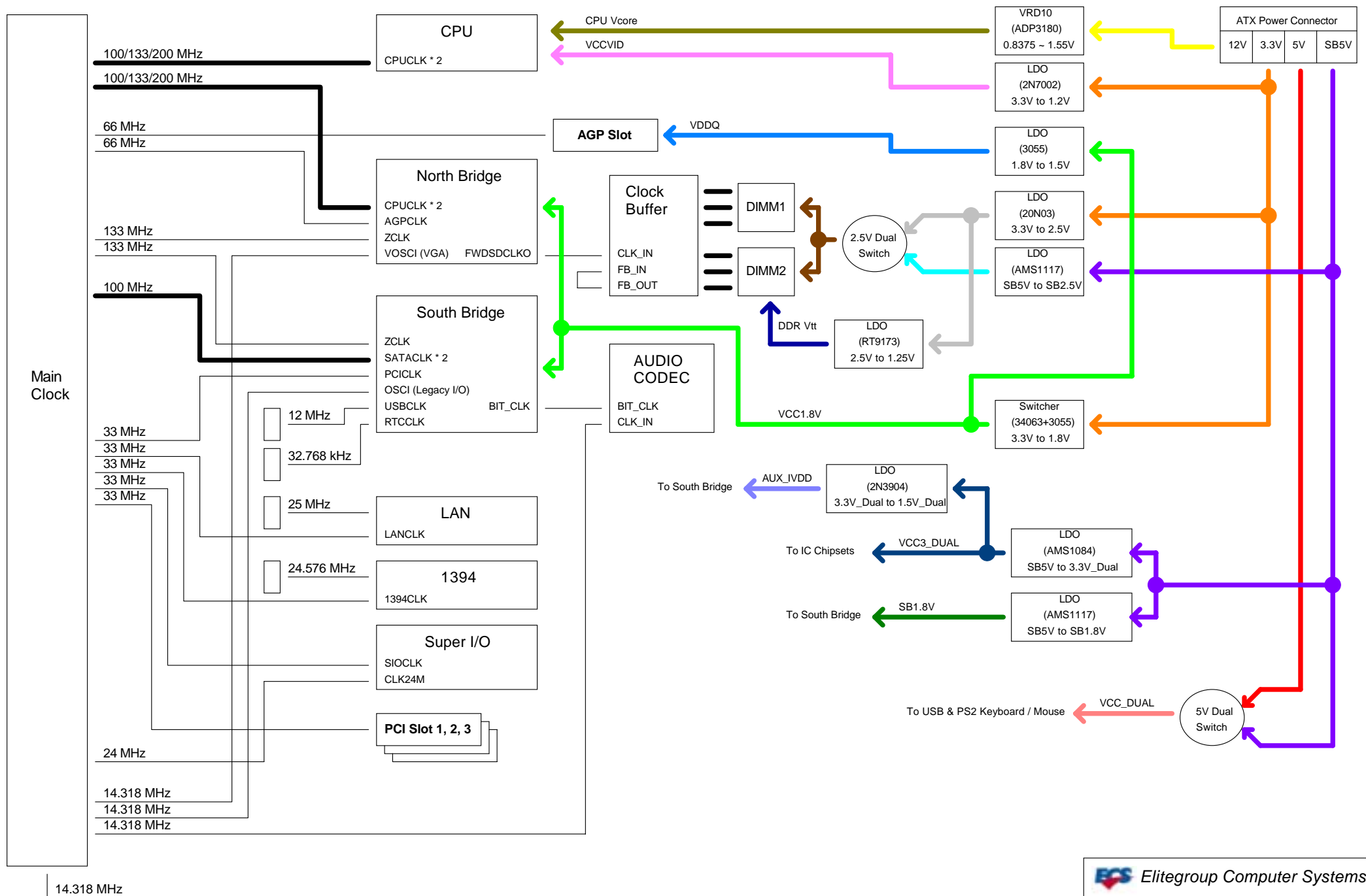
**LAYOUT**

**CHECK**

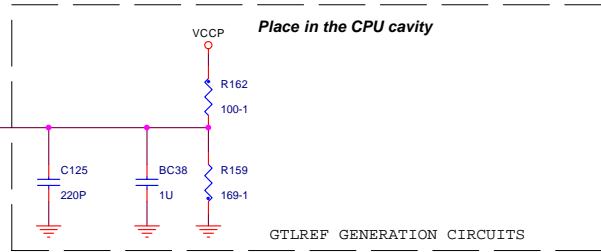
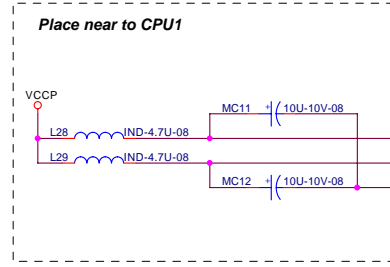
**APPROVAL**

 Elitegroup Computer Systems			
Title <b>SF2 / 661FX</b>			
Size	Document Number		Rev
Custom	Cover Sheet		1.0
Date	Friday, September 12, 2003		Sheet 1 of 36



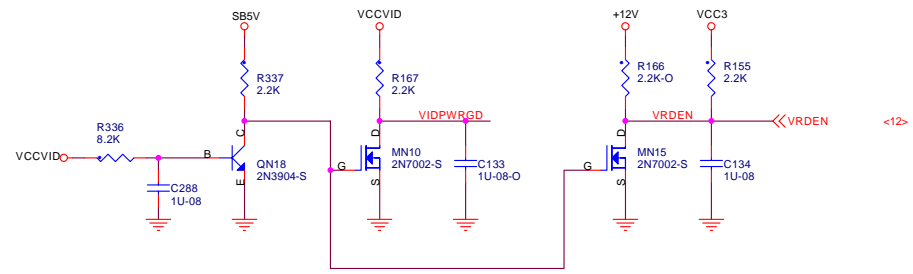
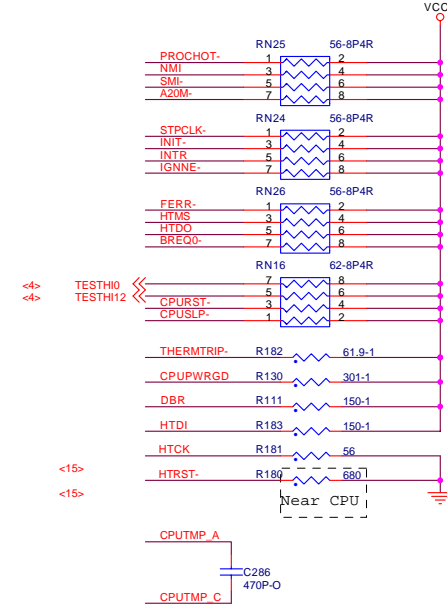
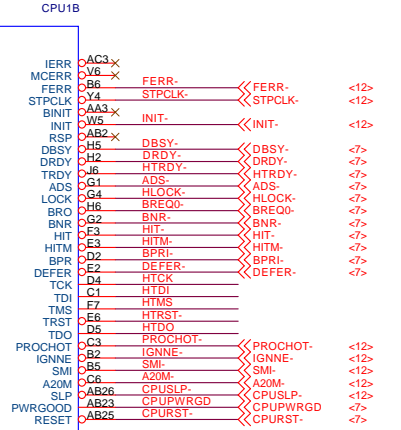
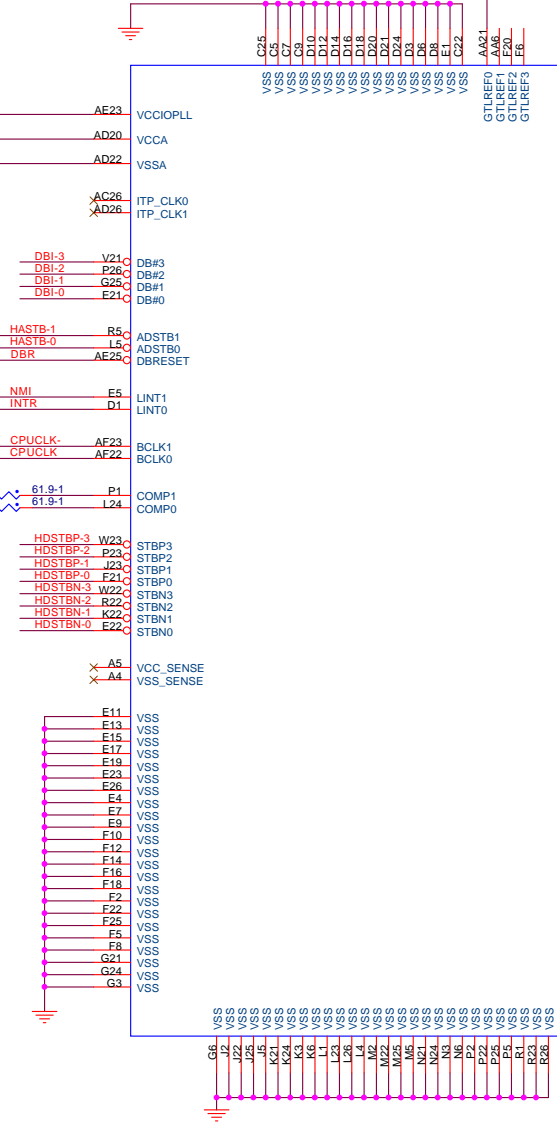




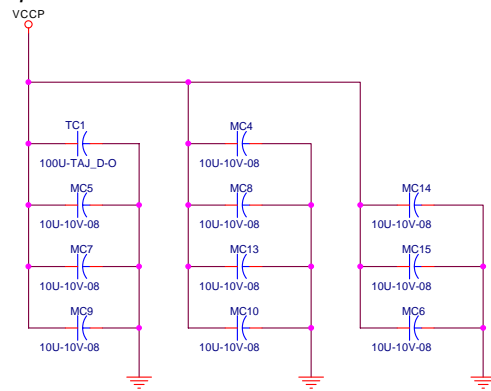


DBI-[0..3] <<DBI-[0..3] <7>  
 HDSTBN-[0..3] <<HDSTBN-[0..3] <7>  
 HDSTBP-[0..3] <<HDSTBP-[0..3] <7>  
 HASTB-[0..1] <<HASTB-[0..1] <7>

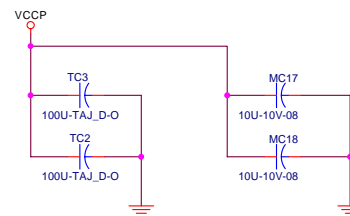
	R173, R164
COMPATIBLE	49.9_1%
OPTIMIZED	61.9_1%



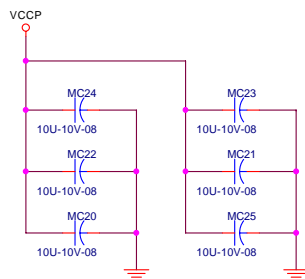
Put these capacitors at processor NORTH SIDE



Put these capacitors INSIDE PROCESSOR CAVITY

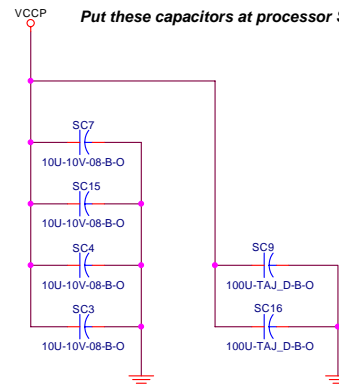


Put these capacitors at processor SOUTH SIDE



P.S. Choose X7R/X5R components instead of Y5V for all 10uF\_1206 capacitors on this page.

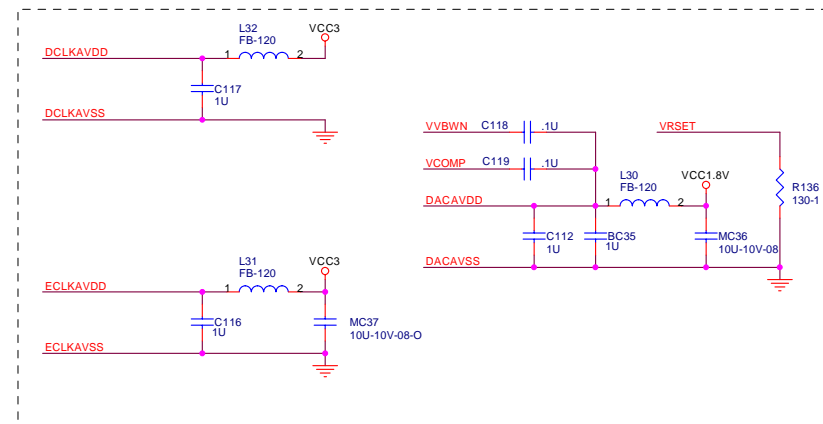
Put these capacitors at processor SOLDER SIDE



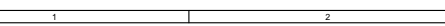
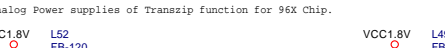
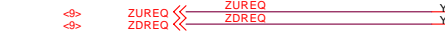
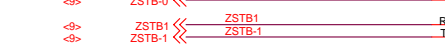
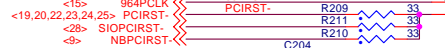
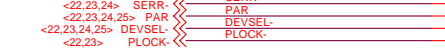
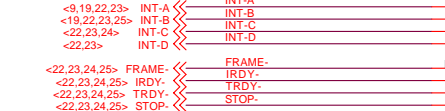
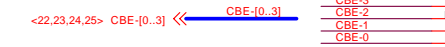
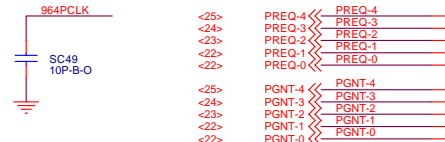
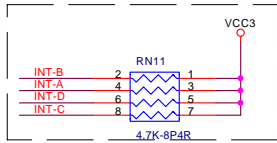












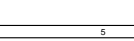
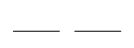
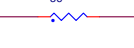
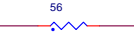
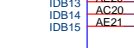
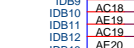
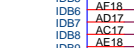
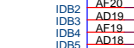
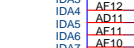
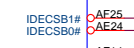
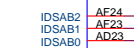
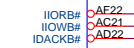
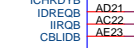
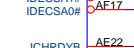
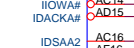
PCI

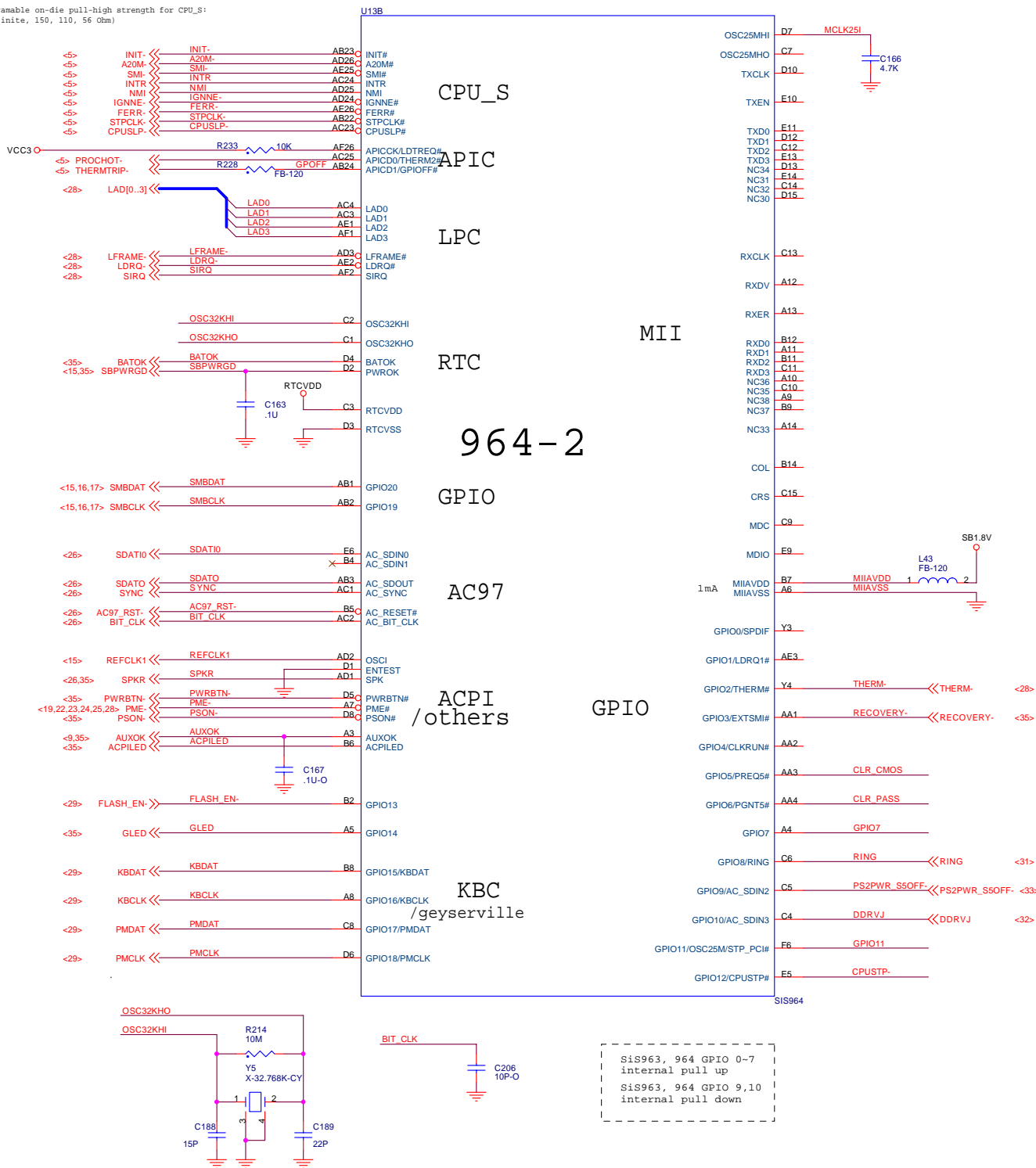
IDE

964-1

HyperZip

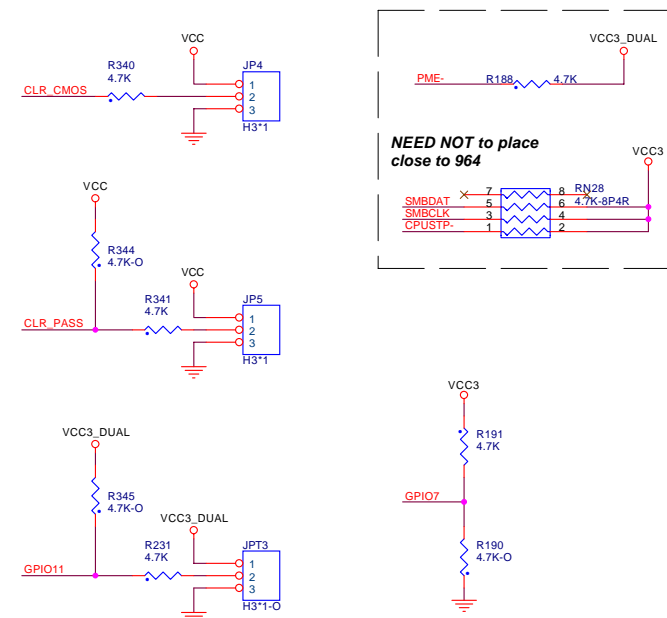
VCC1.8V

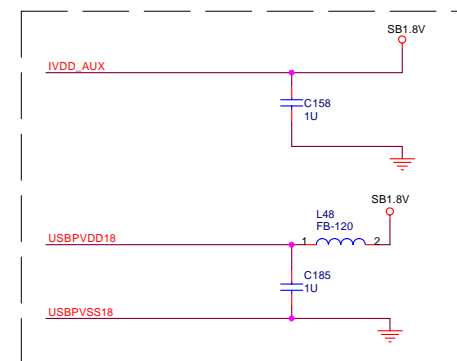
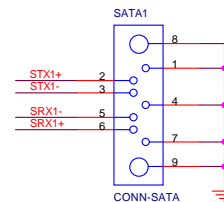
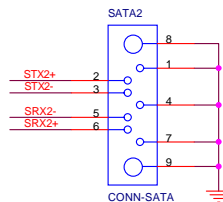
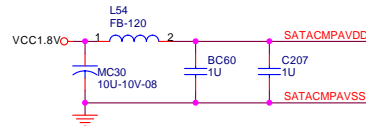
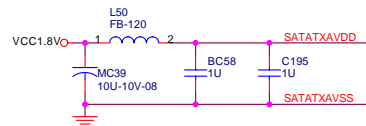
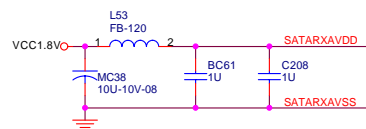
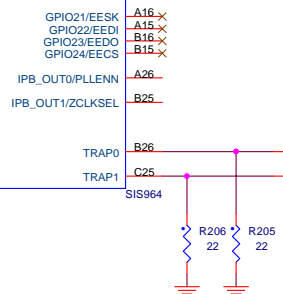
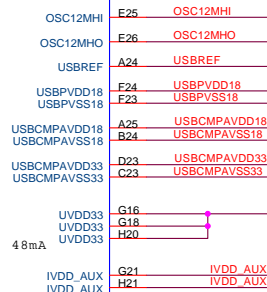
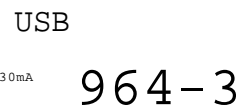
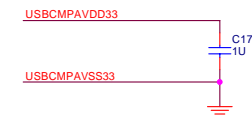
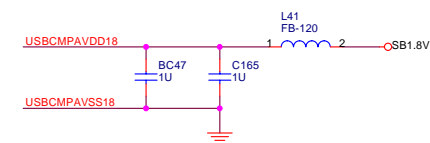
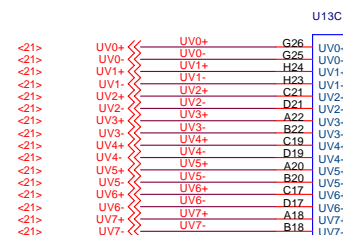


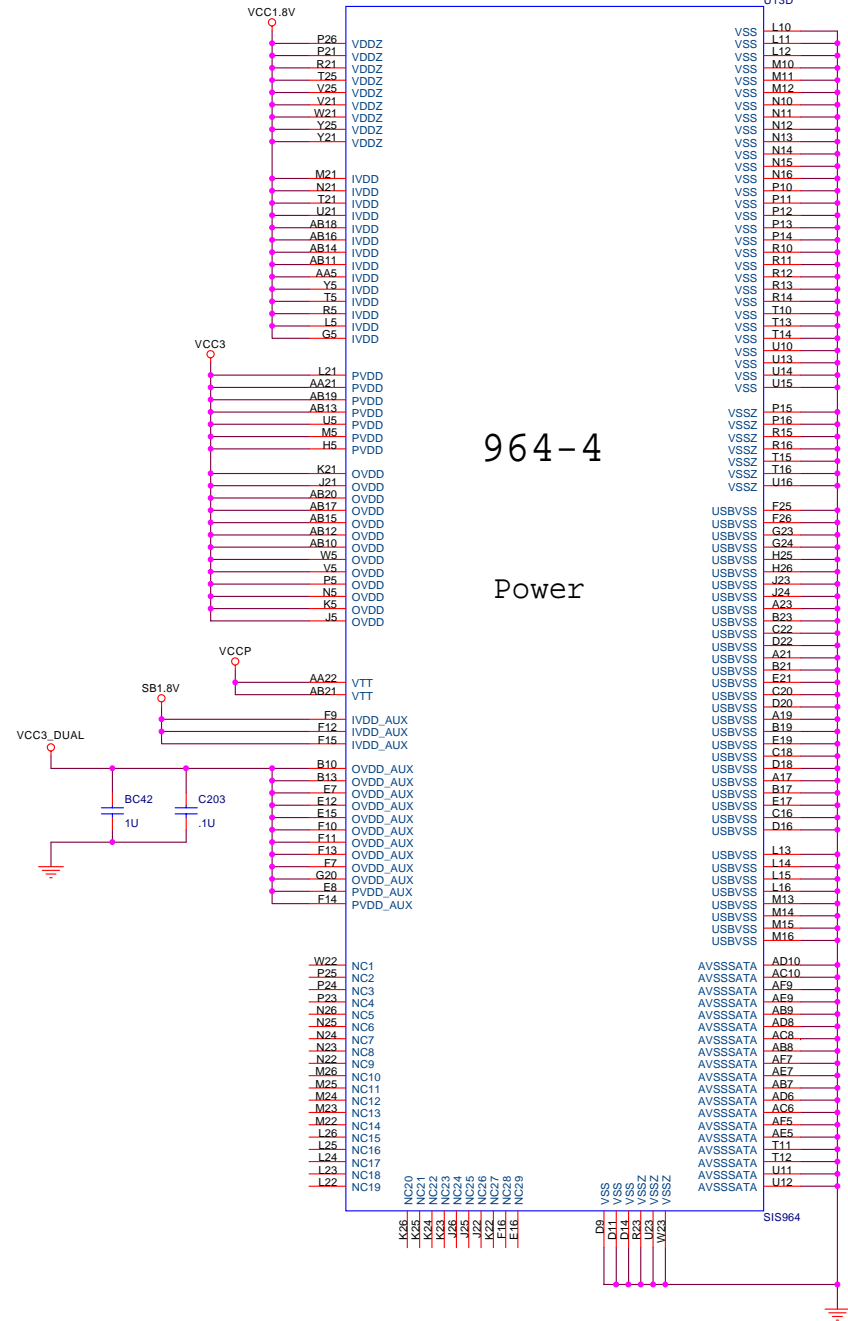
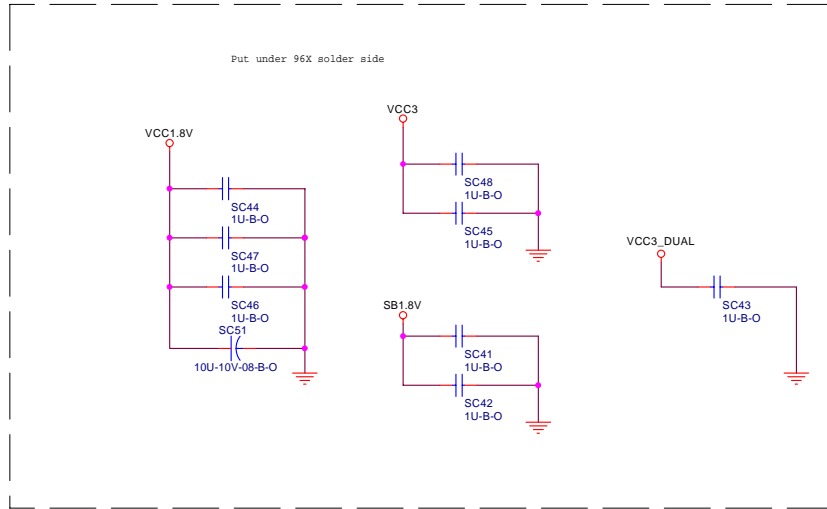
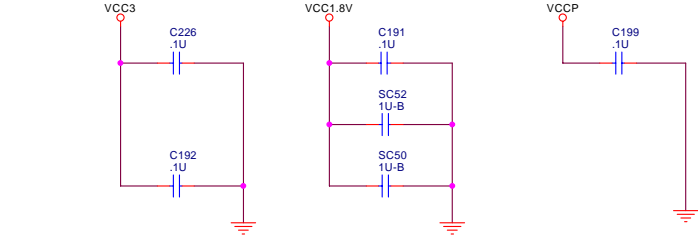


<i>JP4</i>		<i>1-2</i>	<i>2-3</i>
<i>HP</i>	<i>Clear CMOS</i>	<i>Normal</i>	<i>Clear</i>
<i>TRIGEM</i>	<i>Suspen Mode</i>	<i>S1 &amp; S3</i>	<i>S1</i>

<i>JP5</i>		<i>1-2</i>	<i>2-3</i>
<i>HP</i>	<i>Clear Password</i>	<i>Normal</i>	<i>Clear</i>
<i>TRIGEM</i>	<i>Logo Jumper</i>	<i>TG</i>	<i>Commaeul</i>



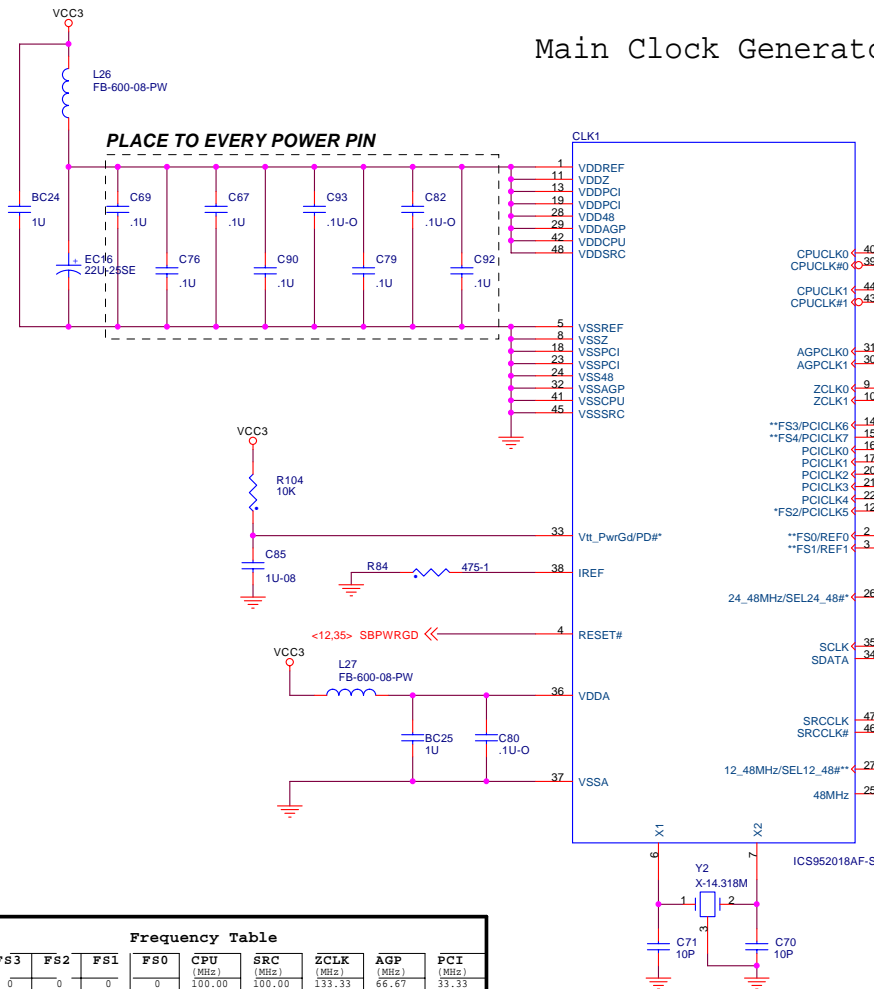




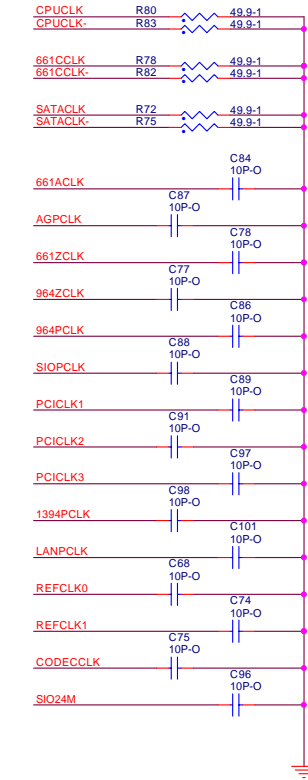
964-4

Power

# Main Clock Generator



## By-Pass Capacitors Place near to the Clock Outputs



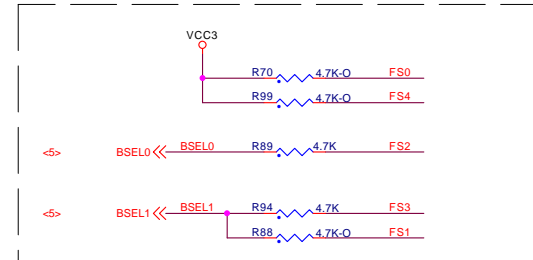
Frequency Table

FS4	FS3	FS2	FS1	FS0	CPU (MHz)	SRC (MHz)	ZCLK (MHz)	AGP (MHz)	PCI (MHz)
0	0	0	0	0	100.00	100.00	133.33	66.67	33.33
0	0	0	0	1	100.99	100.99	134.65	67.33	33.66
0	0	0	1	0	103.00	103.00	137.33	68.67	34.33
0	0	0	1	1	100.00	100.00	133.33	66.67	33.33
0	0	1	0	0	133.33	100.00	133.33	66.66	33.33
0	0	1	0	1	134.65	100.99	134.65	67.32	33.66
0	0	1	1	0	137.33	103.00	137.33	68.66	34.33
0	0	1	1	1	133.33	100.00	133.33	66.67	33.33
0	1	0	0	0	200.00	100.00	133.33	66.67	33.33
0	1	0	0	1	201.98	100.99	134.65	67.33	33.66
0	1	0	1	0	206.00	103.00	137.33	68.67	34.33
0	1	0	1	1	200.00	100.00	133.33	66.67	33.33
0	1	1	0	0	166.66	125.00	125.00	66.66	33.33
0	1	1	0	1	168.31	126.23	126.23	67.32	33.66
0	1	1	1	0	171.66	128.74	128.74	68.66	34.33
0	1	1	1	1	166.66	125.00	125.00	66.66	33.33

Frequency Table

FS4	FS3	FS2	FS1	FS0	CPU (MHz)	SRC (MHz)	ZCLK (MHz)	AGP (MHz)	PCI (MHz)
1	0	0	0	0	105.00	105.00	140.00	70.00	35.00
1	0	0	0	1	107.00	107.00	142.67	71.33	35.67
1	0	0	1	0	109.00	109.00	145.33	72.67	36.33
1	0	0	1	1	110.00	110.00	146.67	73.33	36.67
1	0	1	0	0	140.00	105.00	140.00	70.00	35.00
1	0	1	0	1	142.66	107.00	142.67	71.33	35.67
1	0	1	1	0	145.33	109.00	145.33	72.66	36.33
1	0	1	1	1	146.66	110.00	146.66	73.33	36.67
1	1	0	0	0	210.00	105.00	140.00	70.00	35.00
1	1	0	0	1	214.00	107.00	142.67	71.33	35.67
1	1	0	1	0	218.00	109.00	145.33	72.67	36.33
1	1	0	1	1	220.00	110.00	146.67	73.33	36.67
1	1	1	0	0	266.66	100.00	133.33	66.67	33.33
1	1	1	0	1	269.33	101.00	134.67	67.33	33.67
1	1	1	1	0	274.66	103.00	137.33	68.67	34.33
1	1	1	1	1	266.66	100.00	133.33	66.67	33.33

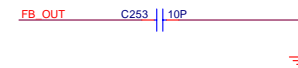
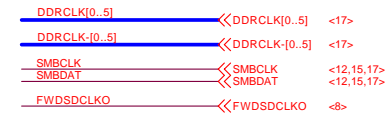
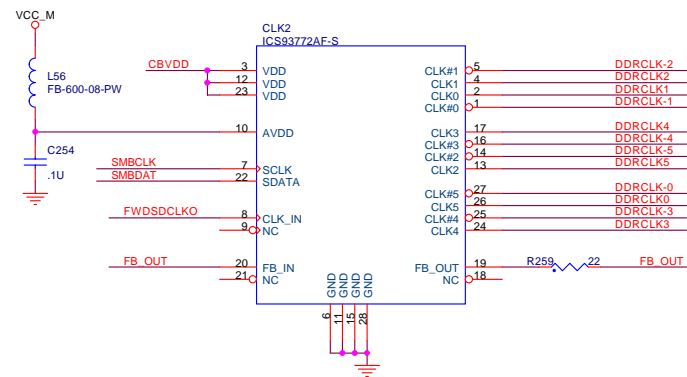
## Frequency Selection



Clock Generator Table	FS4	FS3	FS2	FS1	FS0
Hardware Trapping	Low	BSEL1	BSEL0	Low	Low
CPU=100 (BSEL[1:0]=00)	0	0	0	0	0
CPU=133 (BSEL[1:0]=01)	0	0	1	0	0
CPU=200 (BSEL[1:0]=10)	0	1	0	0	0

Elitegroup Computer Systems

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( 5 OPTIONS)
1: (ICS) ICS93716
2: (Winbond)
3: (ICWorks)
4: (IMI)
5: (AMI)
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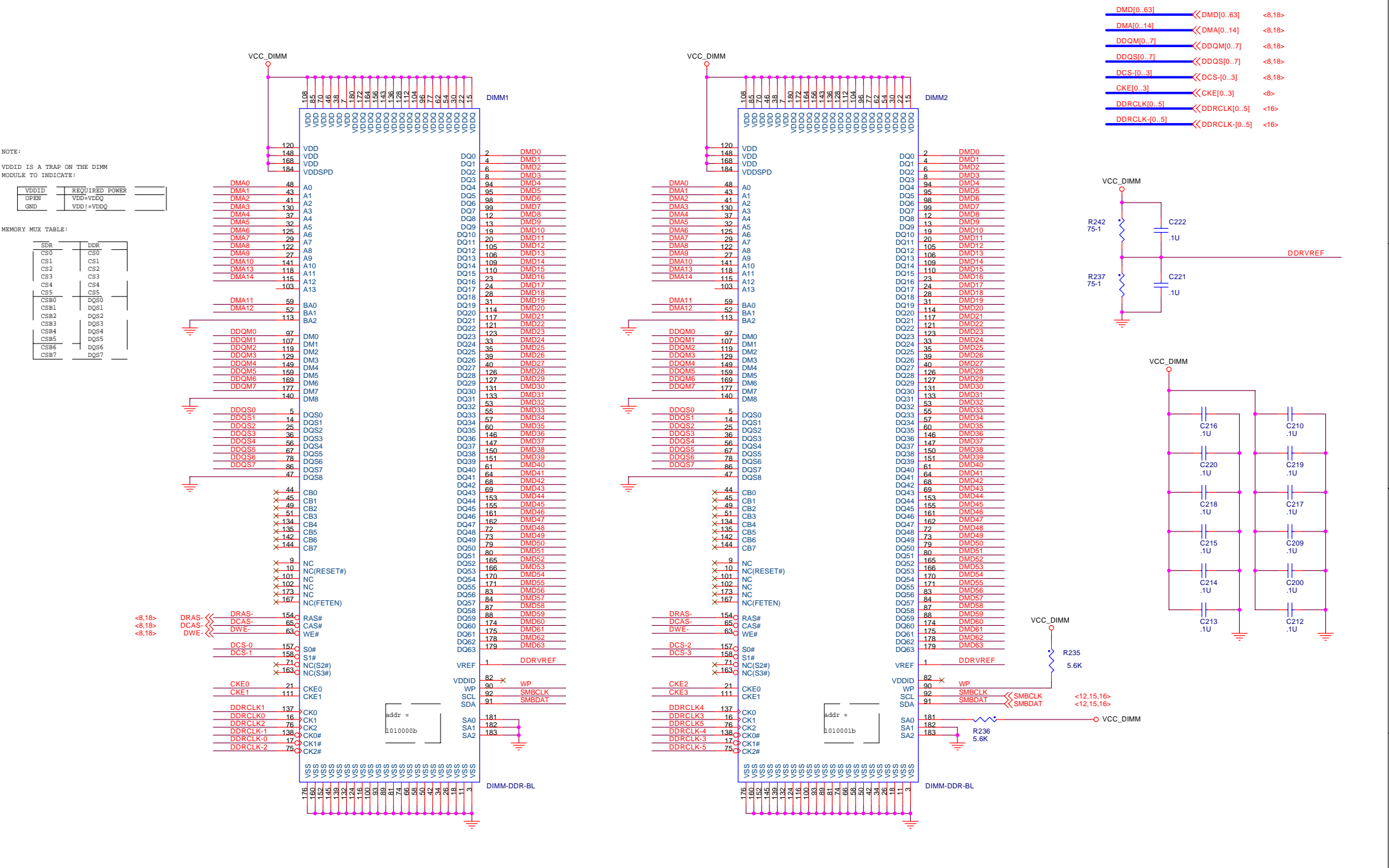


NOTE:  
VDDID IS A TRAP ON THE DIMM  
MODULE TO INDICATE:

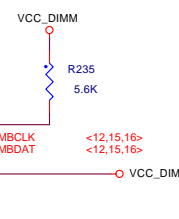
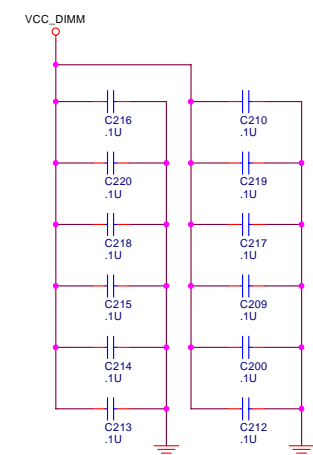
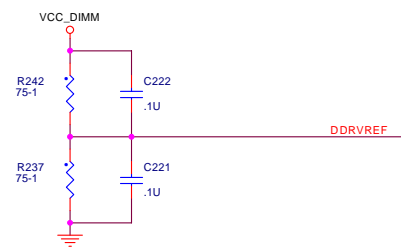
VDDID	REQUIRED POWER
OPEN	VDD=VDDQ
GND	VDD!=VDDQ

MEMORY MUX TABLE:

SDR	DDR
CS0	CS0
CS1	CS1
CS2	CS2
CS3	CS3
CS4	CS4
CS5	CS5
CSB0	DQS0
CSB1	DQS1
CSB2	DQS2
CSB3	DQS3
CSB4	DQS4
CSB5	DQS5
CSB6	DQS6
CSB7	DQS7

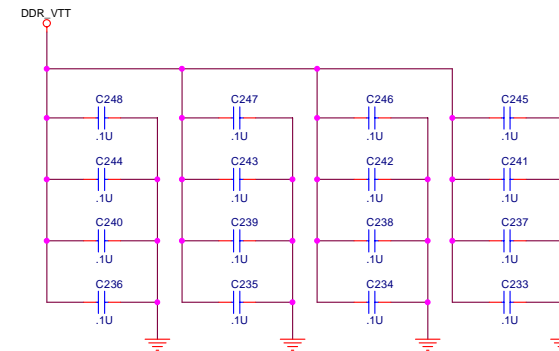
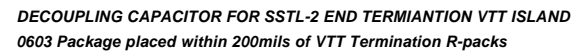


DMD[0..63] << DMD[0..63] <-8,18>  
DMA[0..14] << DMA[0..14] <-8,18>  
DDQM[0..7] << DDQM[0..7] <-8,18>  
DDQS[0..7] << DDQS[0..7] <-8,18>  
DCS[0..3] << DCS[0..3] <-8,18>  
CKE[0..3] << CKE[0..3] <-8>  
DDRCLK[0..5] << DDRCLK[0..5] <-16>  
DDRCLK[0..5] << DDRCLK[0..5] <-16>



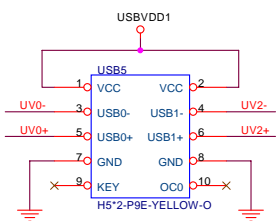
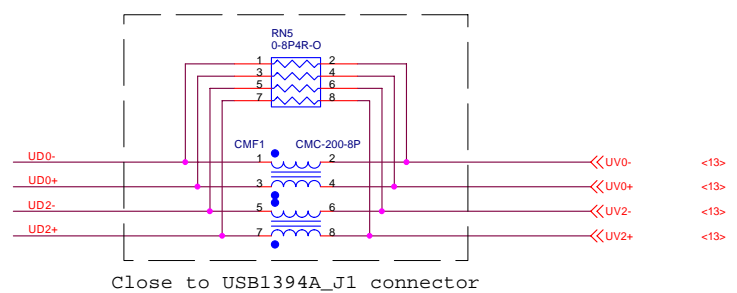
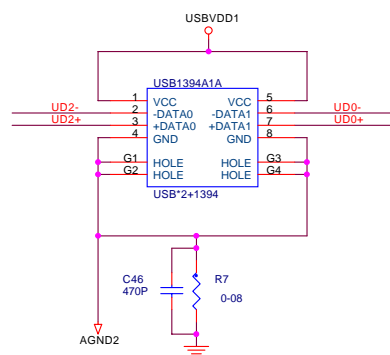
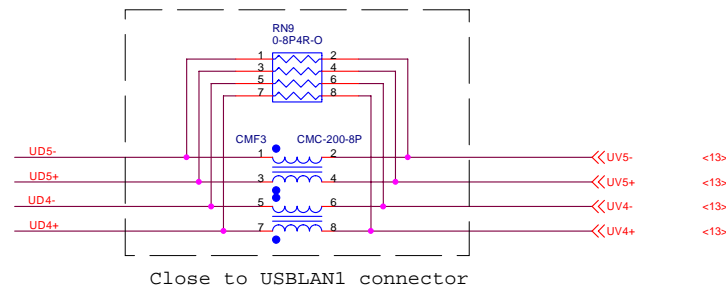
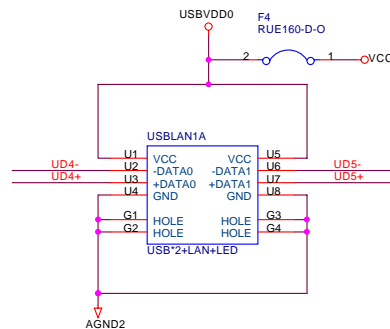
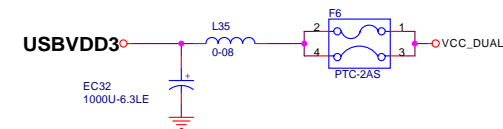
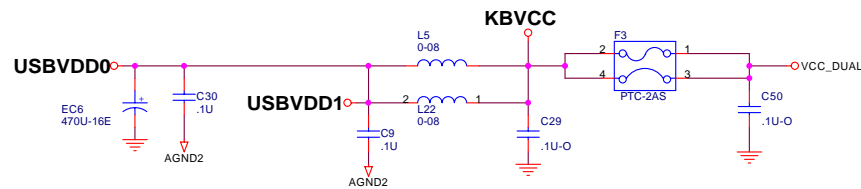
DMD[0..63]	⟨⟨DMD[0..63]	<8,17>
DMA[0..14]	⟨⟨DMA[0..14]	<8,17>
DDQM[0..7]	⟨⟨DDQM[0..7]	<8,17>
DDQS[0..7]	⟨⟨DDQS[0..7]	<8,17>
DCS-[0..3]	⟨⟨DCS-[0..3]	<8,17>

SDR		R <sub>in</sub>	DDR		R <sub>in</sub>	R <sub>tt</sub>
MD/DQM (/DQS)	LV-CMOS	0/10-	STTL-2		1.0	33
MA/Control	LV-CMOS	1.0	STTL-2		0	33
CS	LV-CMOS	0	STTL-2		0	47
CKE	DD 3.3V		DD 2.5V			

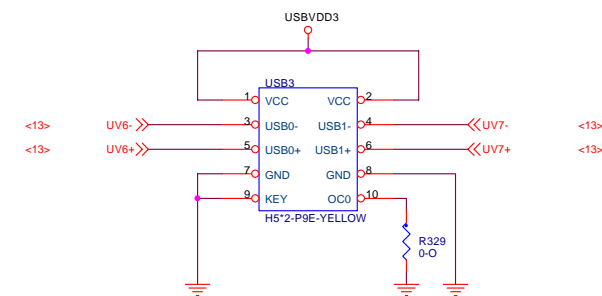
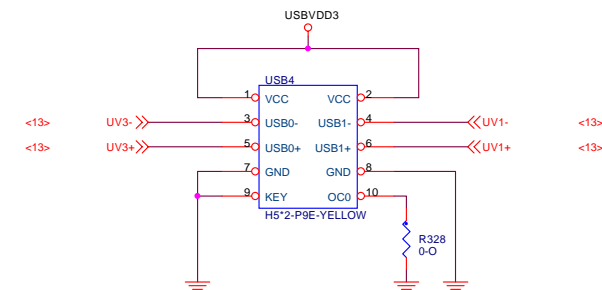




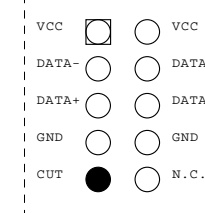




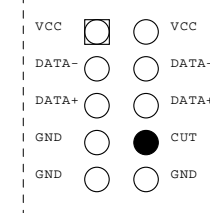
	USB port
Control 0	0, 3, 6
Control 1	1, 4, 7
Control 2	2, 5



Intel USB Header

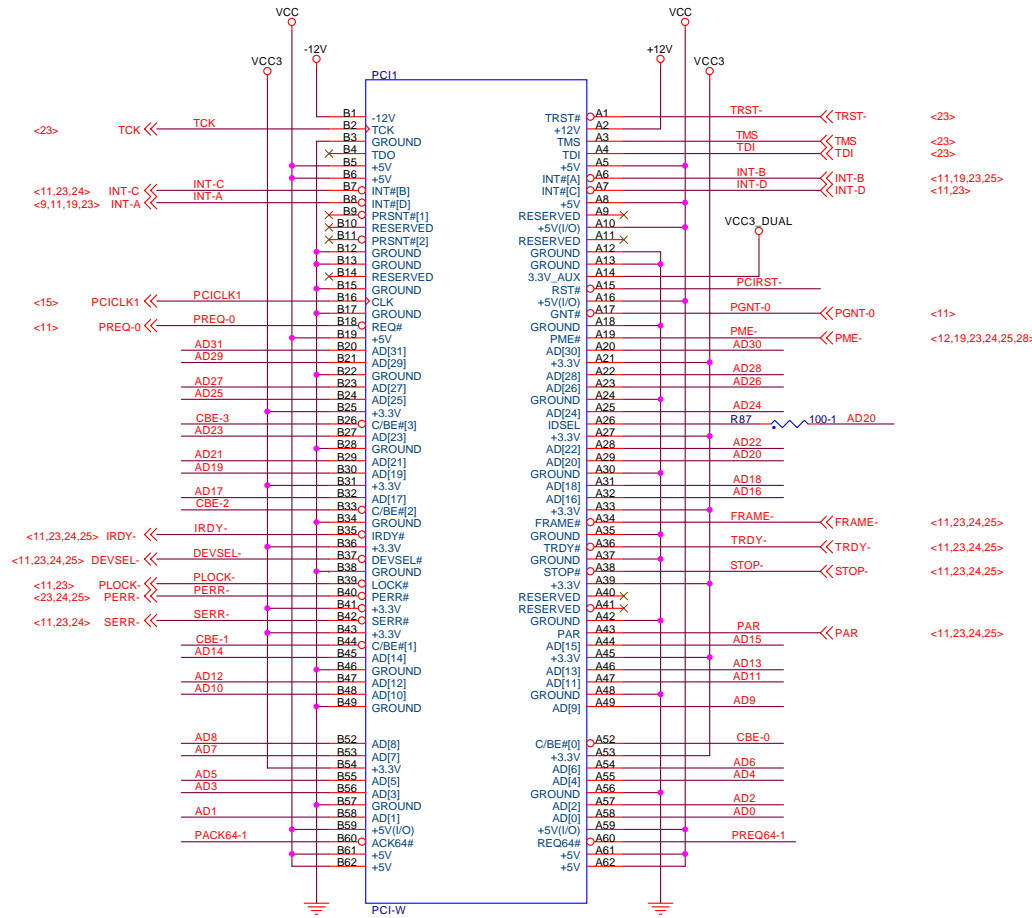


ACER USB Header

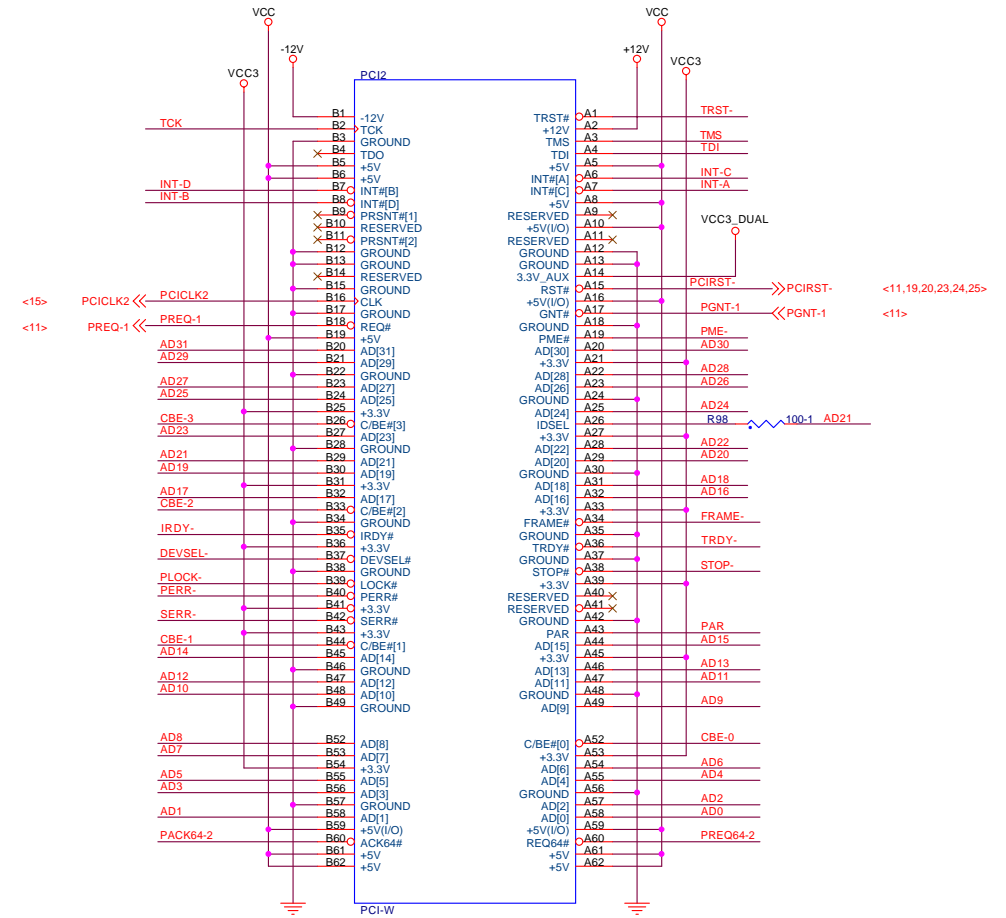


# PCI Slot 1 & 2

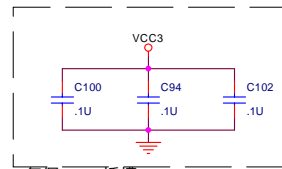
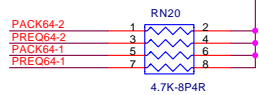
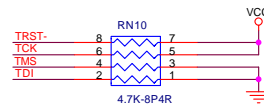
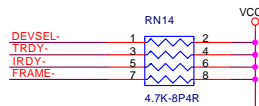
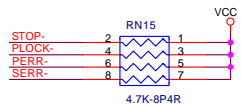
<11,23,24,25> CBE-[0..3] << CBE-[0..3]  
<11,23,24,25> AD[0..31] << AD[0..31]



IDSEL=AD20  
INT[B,C,D,A]



IDSEL=AD21  
INT[C,D,A,B]



每個 PCI 插槽 pin A33  
各放一顆

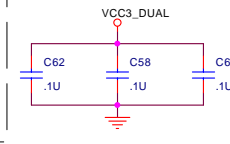
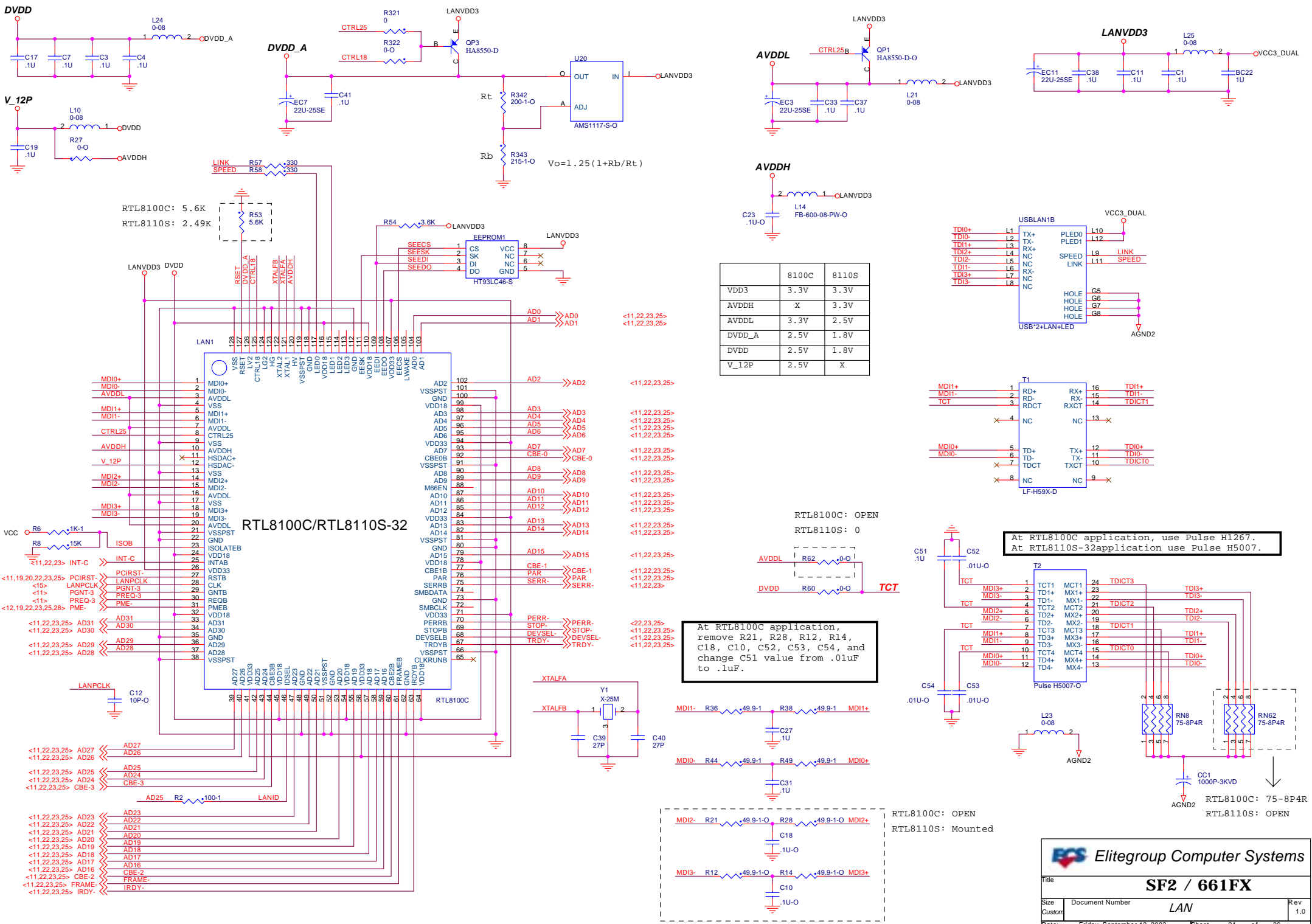




Diagram of the RN21 component, showing its internal structure and connections. The component is labeled RN21 and 4.7K-8P4R. It has eight pins: 1, 3, 5, 7 on the left and 2, 4, 6, 8 on the right. The left pins are connected to PREQ64-3 and PACK64-3. The right pins are connected to VCC.

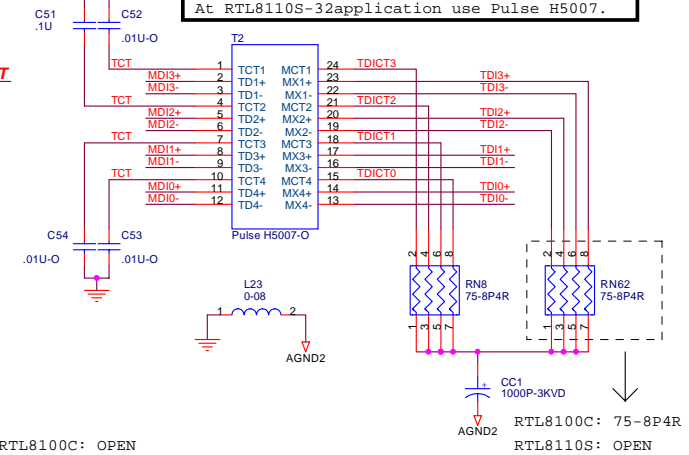


	8100C	8110S
VDD3	3.3V	3.3V
AVDDH	X	3.3V
AVDDL	3.3V	2.5V
DVDD_A	2.5V	1.8V
DVDD	2.5V	1.8V
V_12P	2.5V	X

RTL8100C: OPEN  
RTL8110S: 0

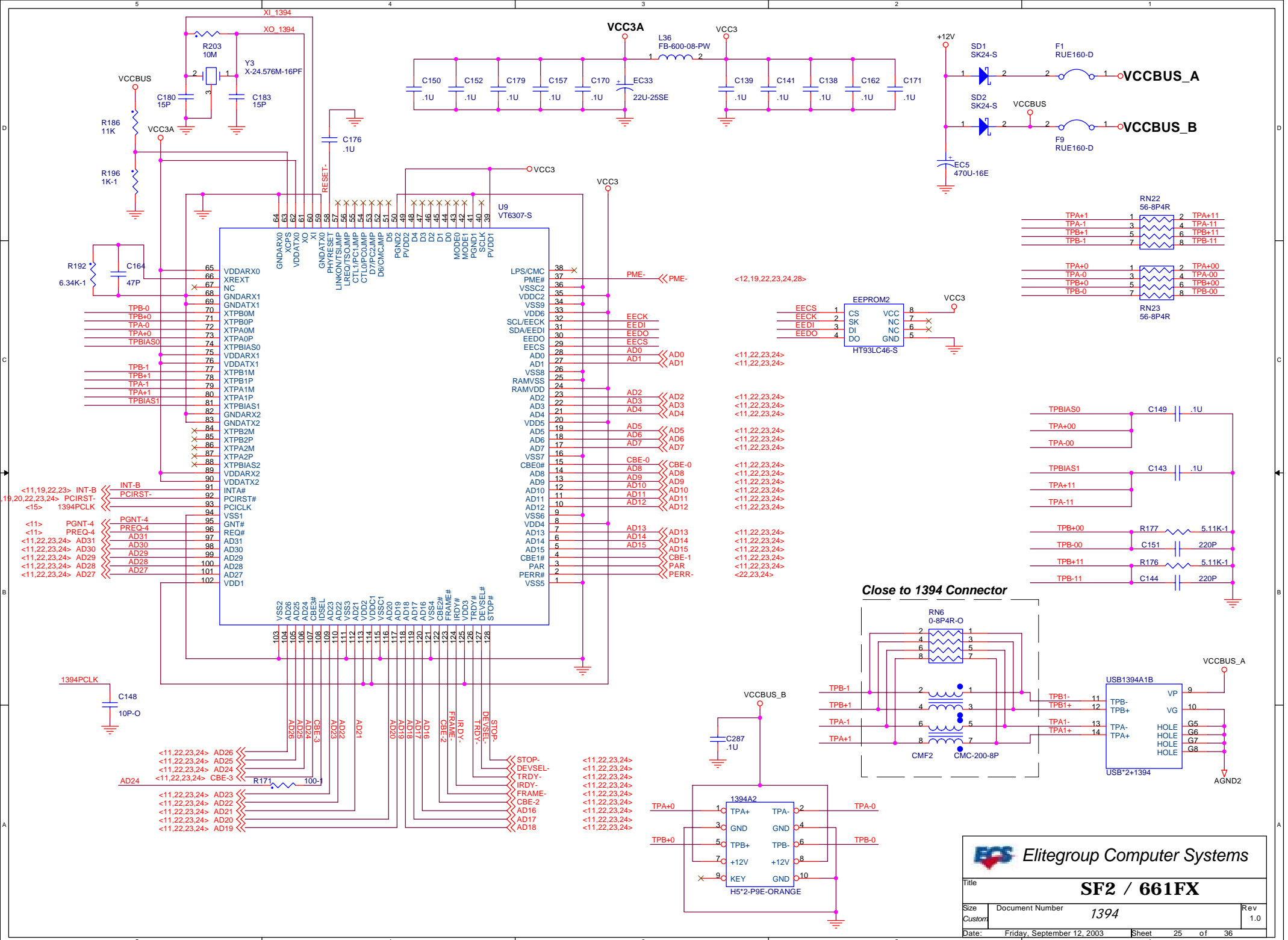
At RTL8100C application,  
remove R21, R28, R12, R14,  
C18, C10, C52, C53, C54, and  
change C51 value from .01uF  
to .1uF.

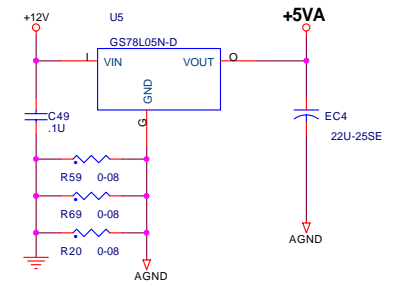
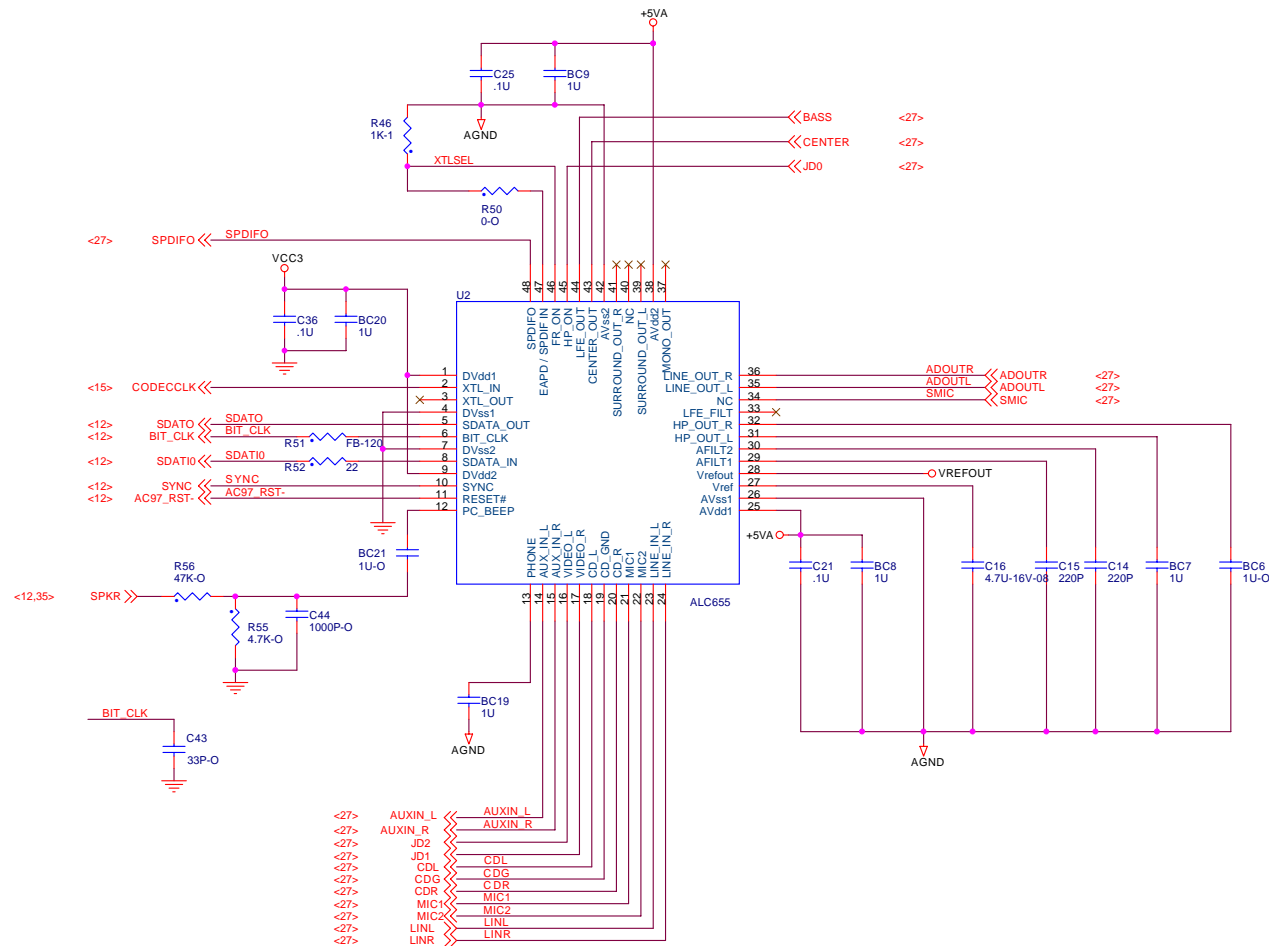
At RTL8100C application, use Pulse H1267.  
At RTL8110S-32 application use Pulse H5007.

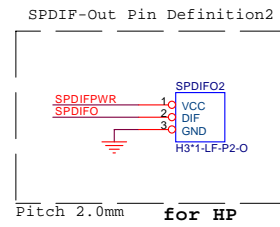
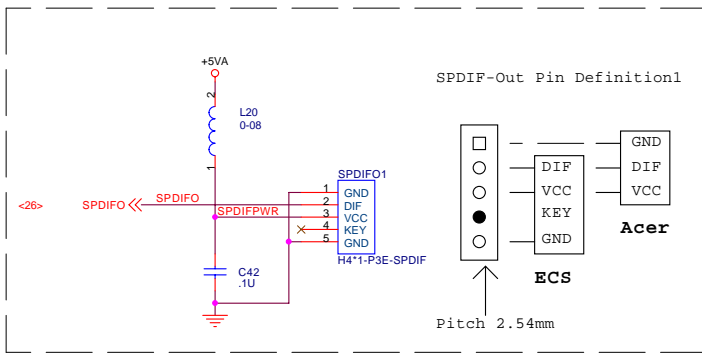
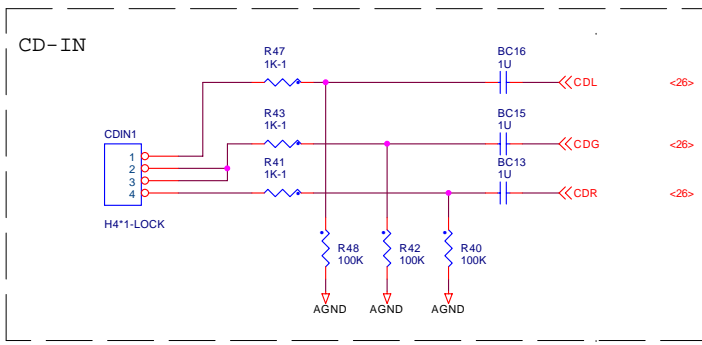
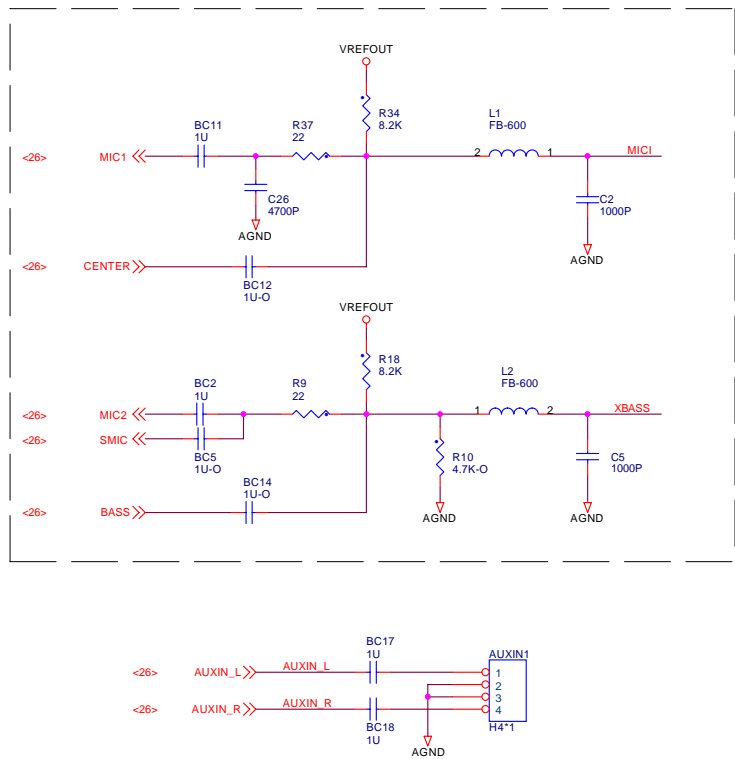
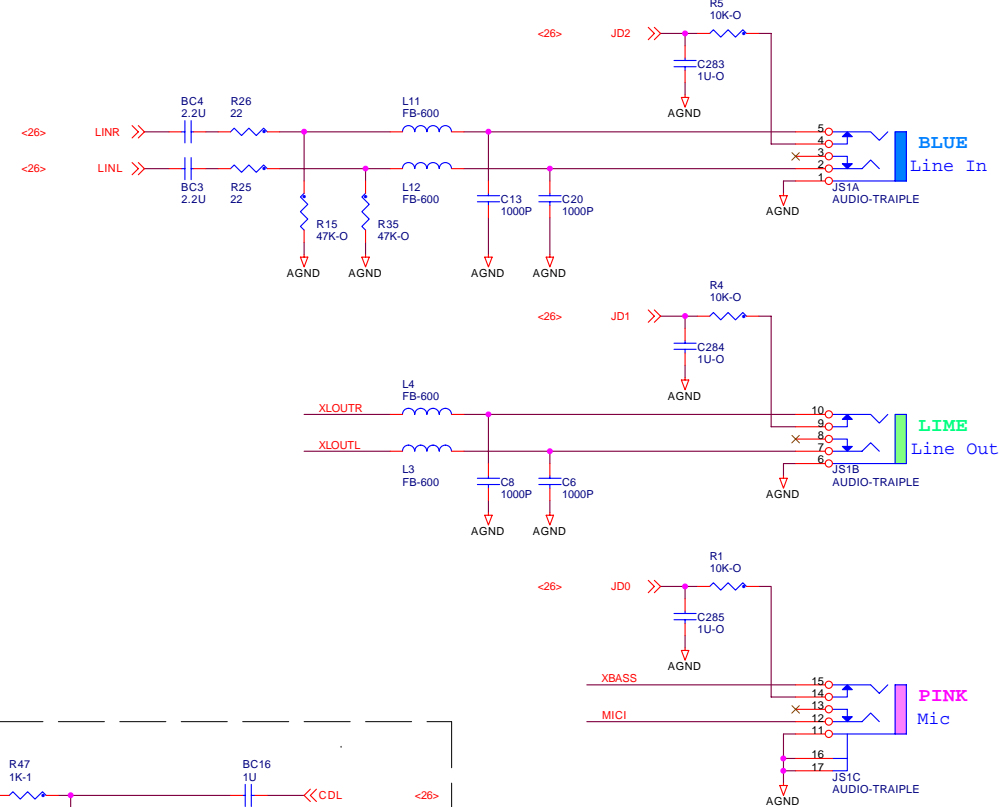
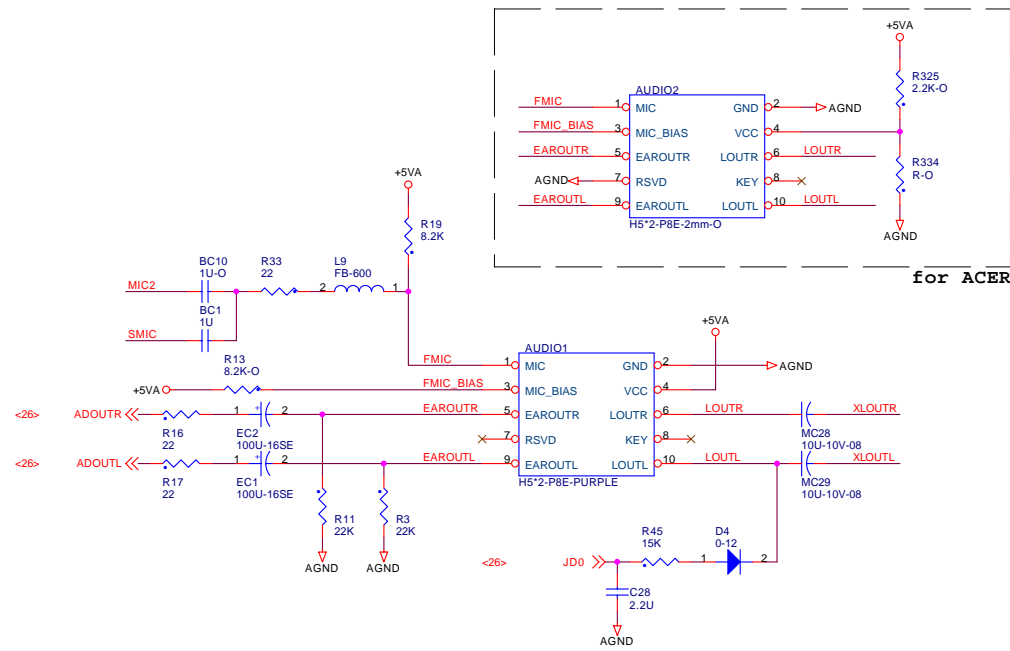


RTL8100C: OPEN  
RTL8110S: Mounted

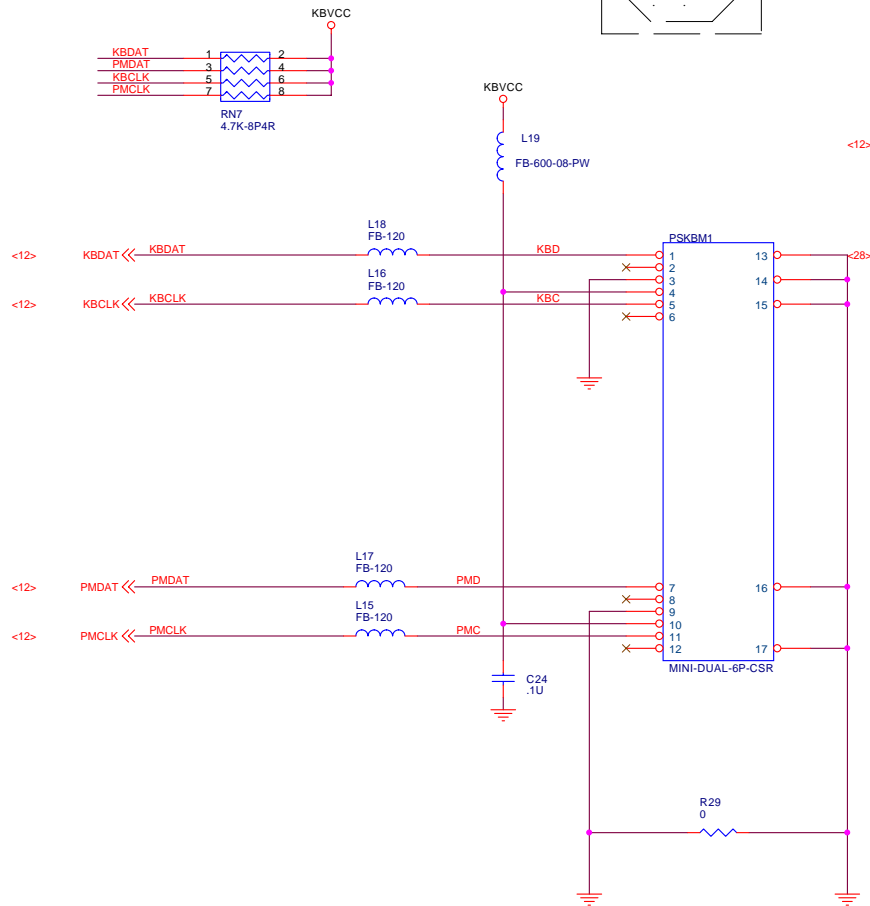
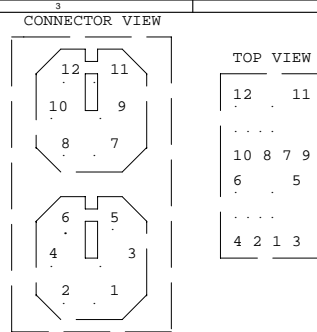




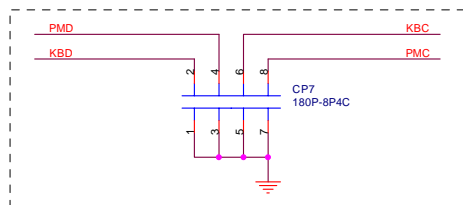




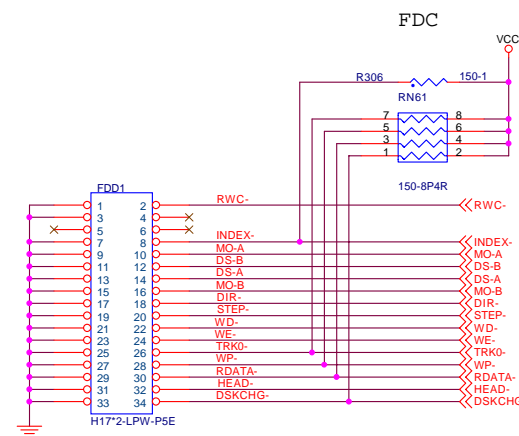
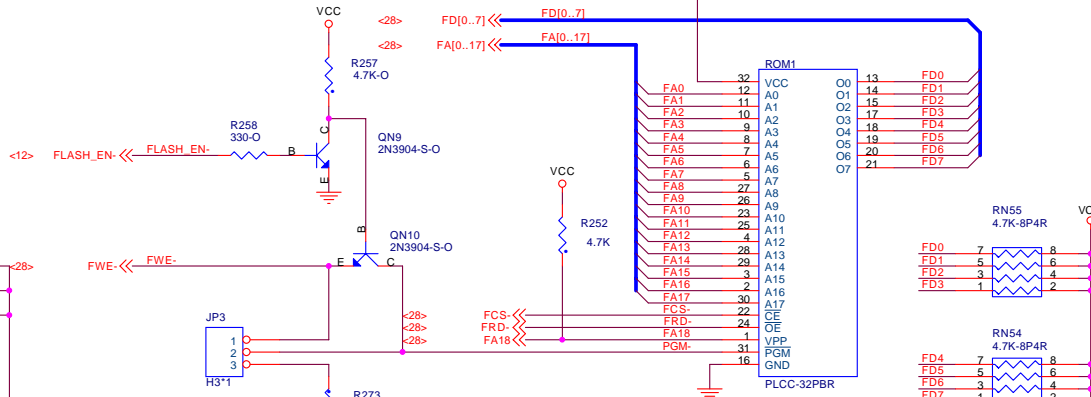


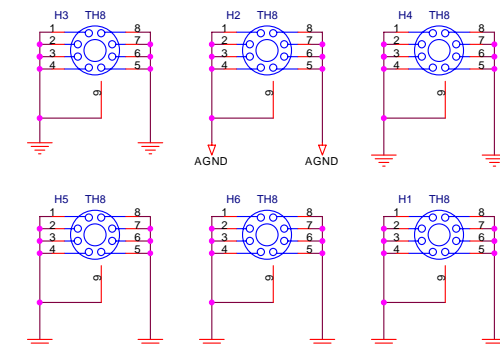
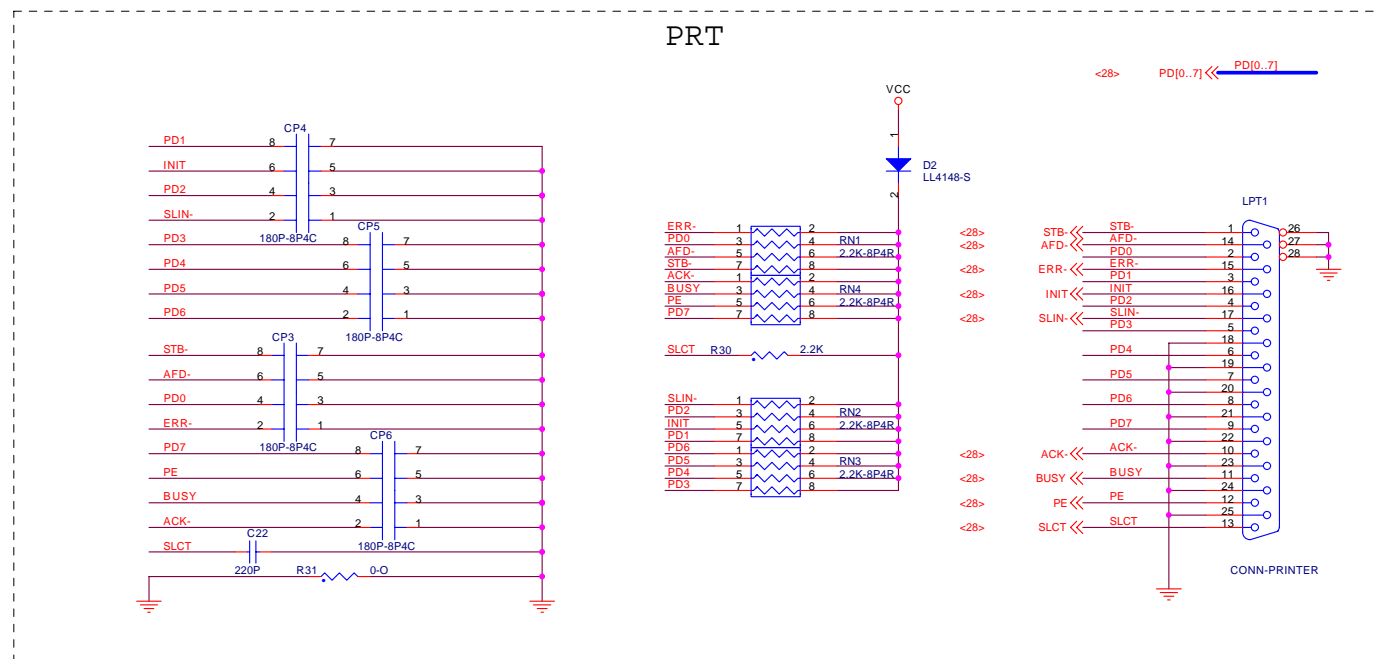
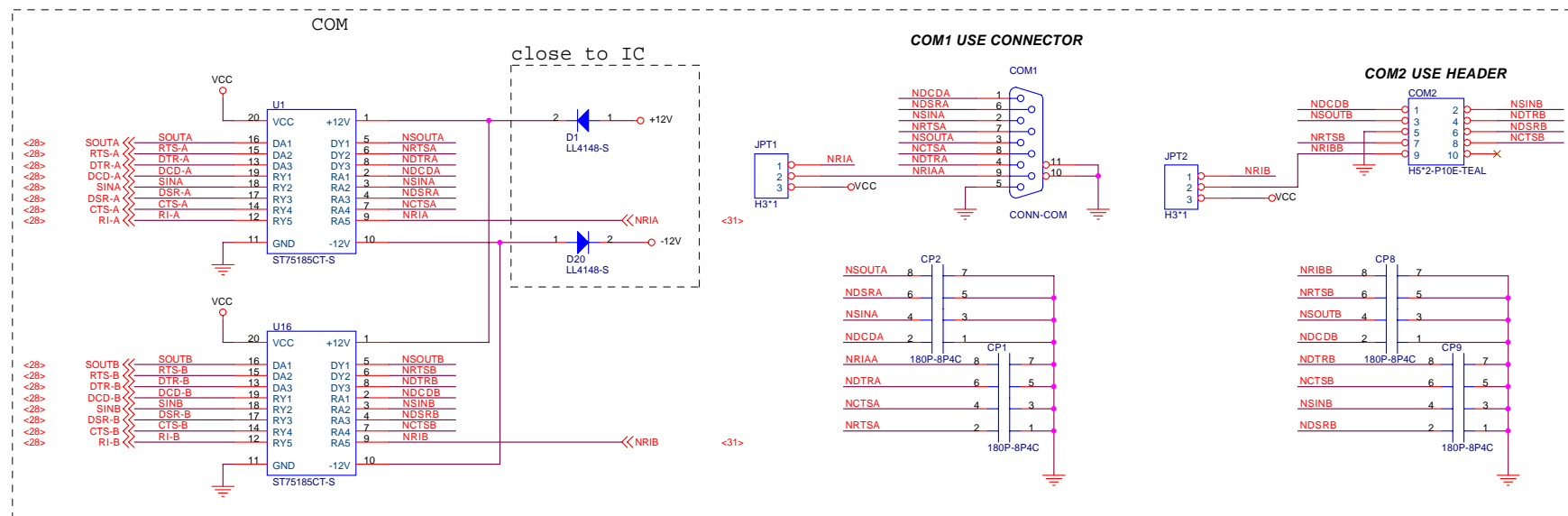


PLACE NEAR CONNECTOR

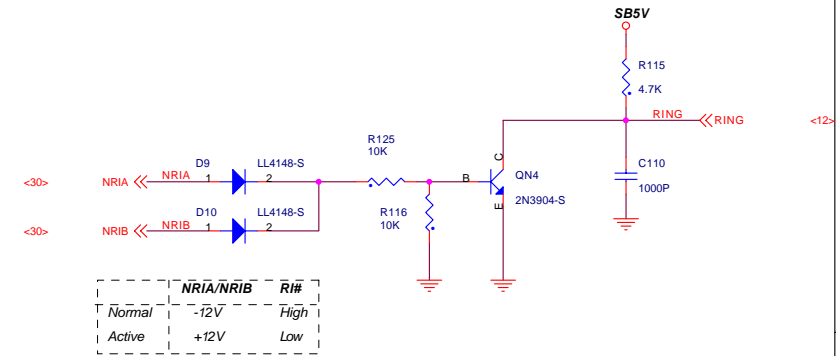
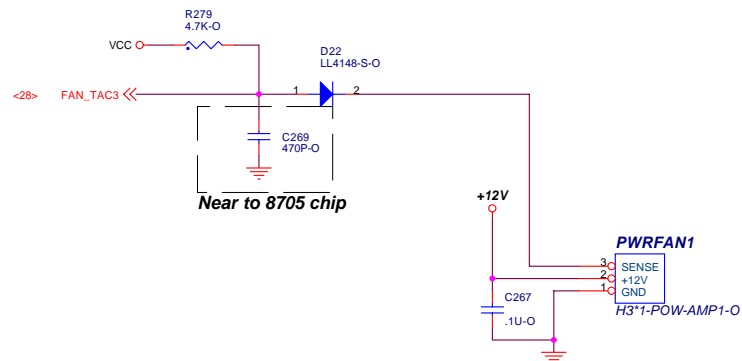
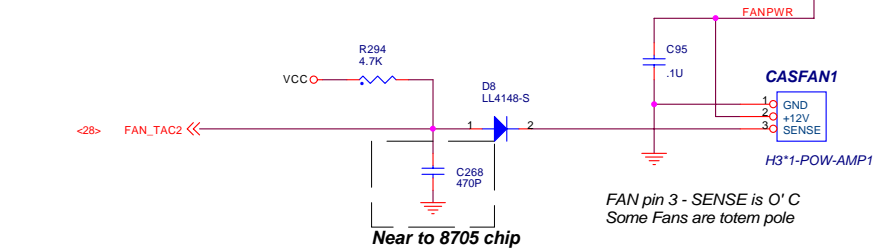
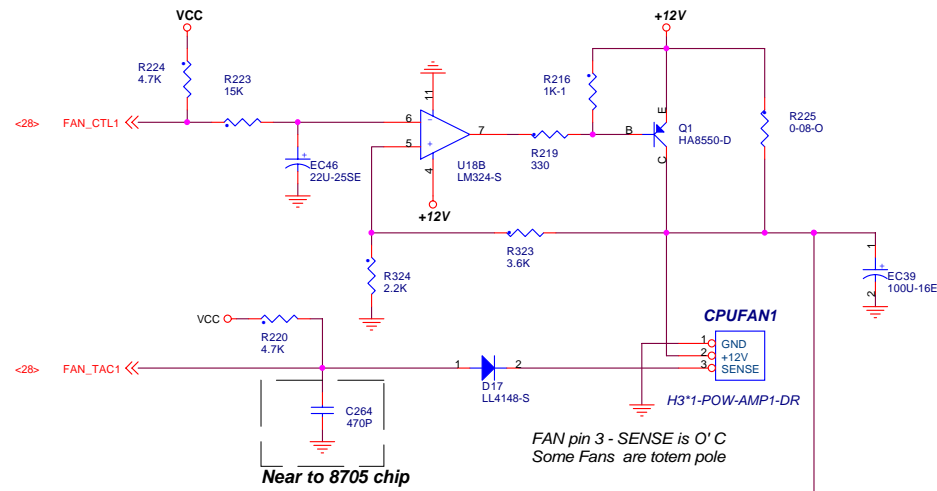


JP3	BIOS PROTECT
1-2	Write Enable
2-3	Write Disable



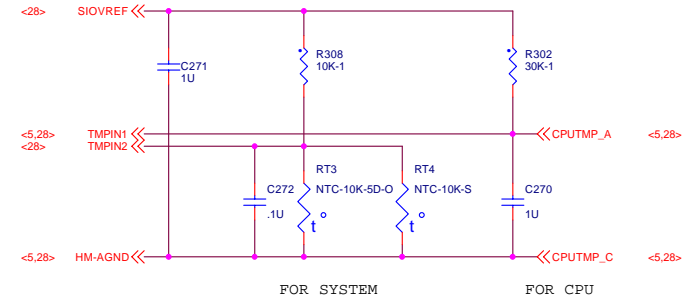


**Layout :**  
Power Signals : CPUFAN, CASEFAN, PWRFAN trace width should > 20 mil with current 200 mA .

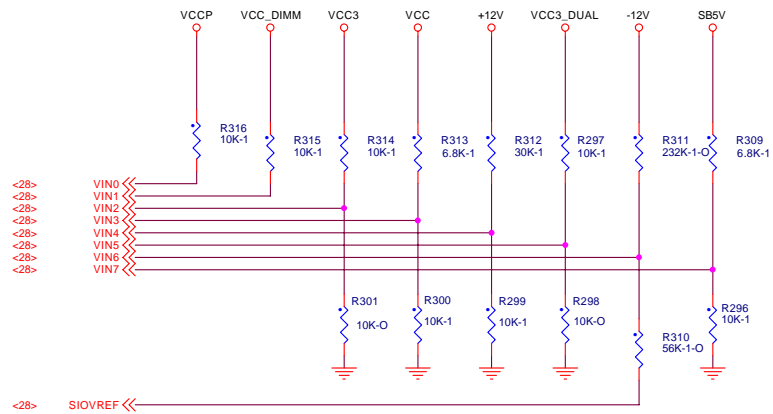


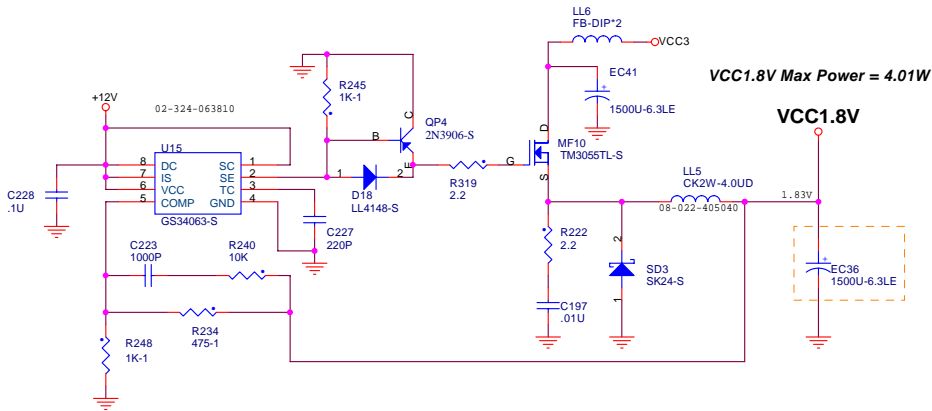
## Temperature Monitor

Choosing method of measuring temperature by either thermistor or diode



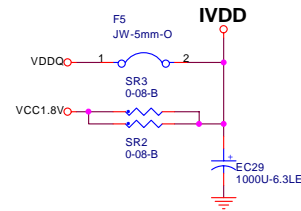
## Voltage Monitor



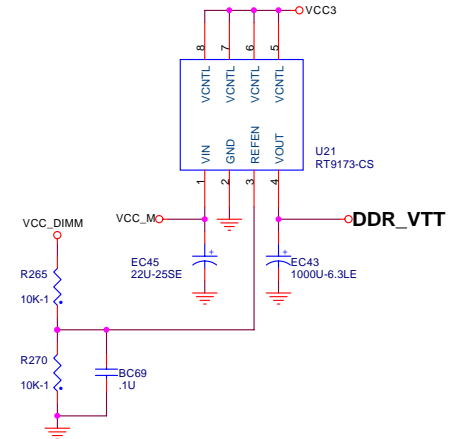


VCC1.8V Max Power = 4.01W

VCC1.8V



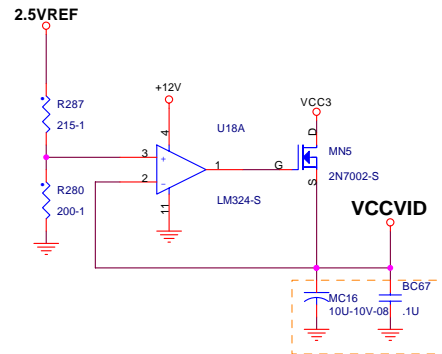
IVDD



DDR\_VTT

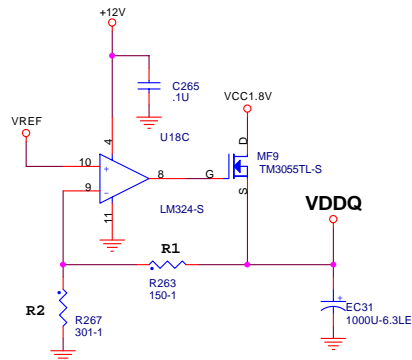
	IVDD	VCC1.8V	
648	1.8V	1.8V	short two power plane, one regulator
648FX	1.9V	1.9V	short two power plane, one regulator
661FX	1.8V	1.8V	short two power plane, one regulator or two regulator
661FXLV	1.5V	1.8V	two regulator

	AUX_IVDD	SB1.8V	
648	1.8V	1.8V	short two power plane, one regulator
648FX	1.9V	1.9V	short two power plane, one regulator
661FX	1.8V	1.8V	short two power plane, one regulator
661FXLV	1.5V	1.8V	two regulator

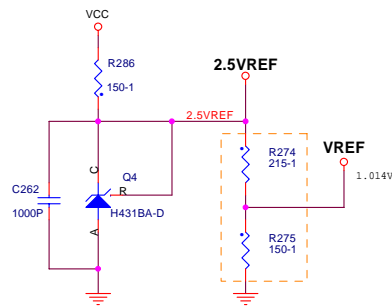


VCCVID

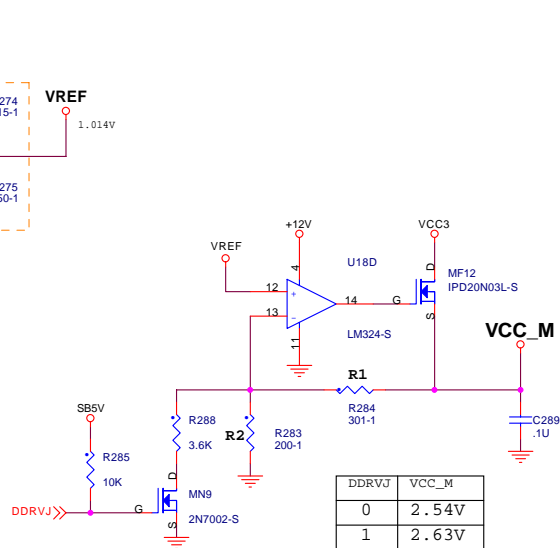
VCC1.5V Max Power = 0.3\*(0.289+2.35)=0.7917W



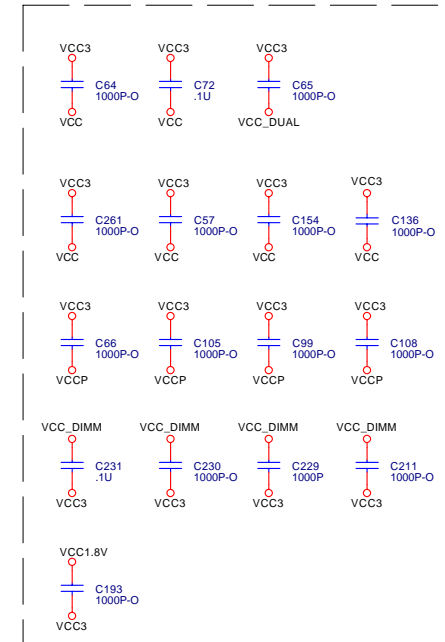
$$V_o = V_{REF} (1 + R_1/R_2)$$



<12>



DDR_VJ	VCC_M
0	2.54V
1	2.63V



平均分佈在POWER PLAN 和 PLAN 之間

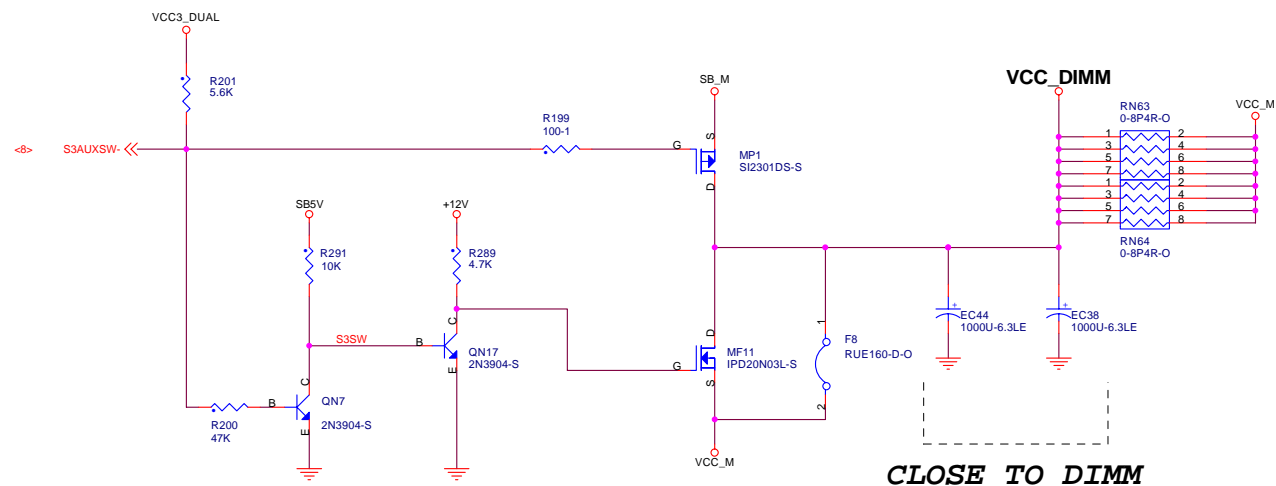
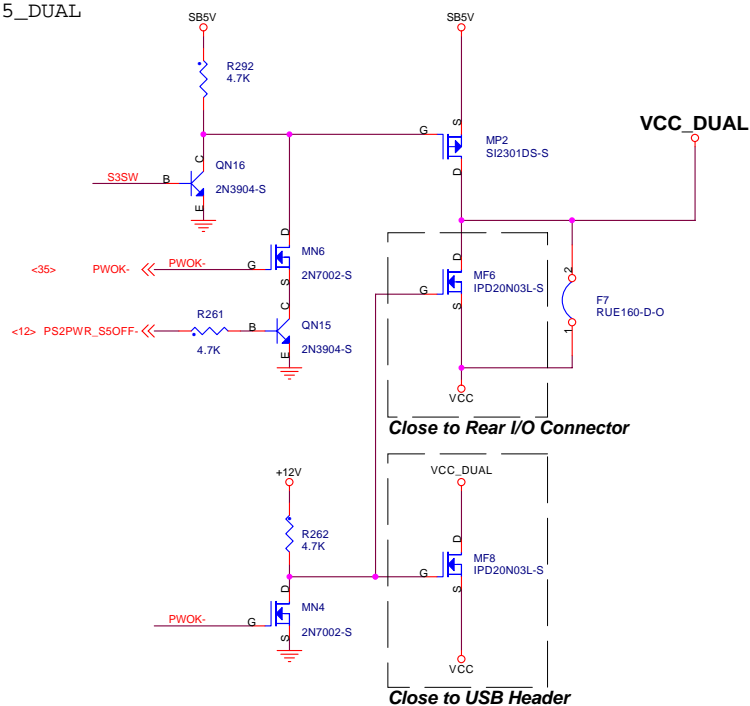


```
1.IN S0,S1
THIS CIRCUIT PASSES THE NORMAL POWER
```

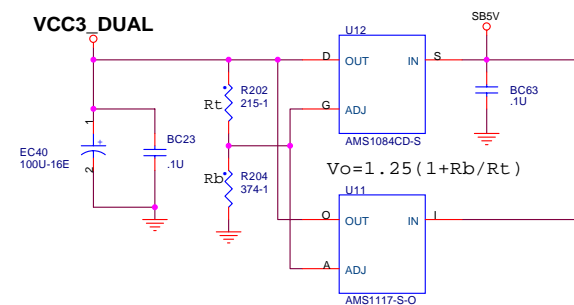
2.IN S3,S4,S5  
THIS CIRCUIT PASSES THE STANDBY POWER.

NOTE:  
BECAUSE OF THE MAXIMUM CURRENT FROM  
POWER SUPPLY IS ONLY ABOUT 750-1000mA  
SO IF YOU WANT TO SUPPORT WAKE UP  
FROM S3 BY USB, YOU MUST HAVE A POWER  
SUPPLY WITH LARGER POWER.(ADDITIONAL  
500mA PER USB PORT)

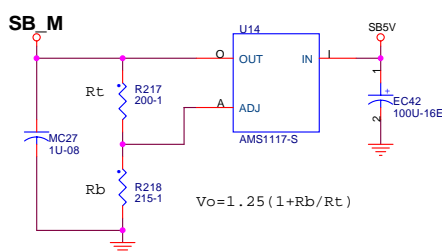
VCC3\_DUAL & VCC5\_DUAL



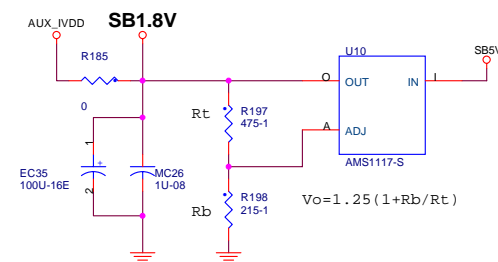
VCC3\_DUAL



## SB\_M

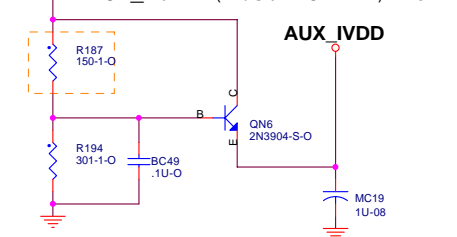


SB1.8V (For SB) 450mA

**SB1.8V**

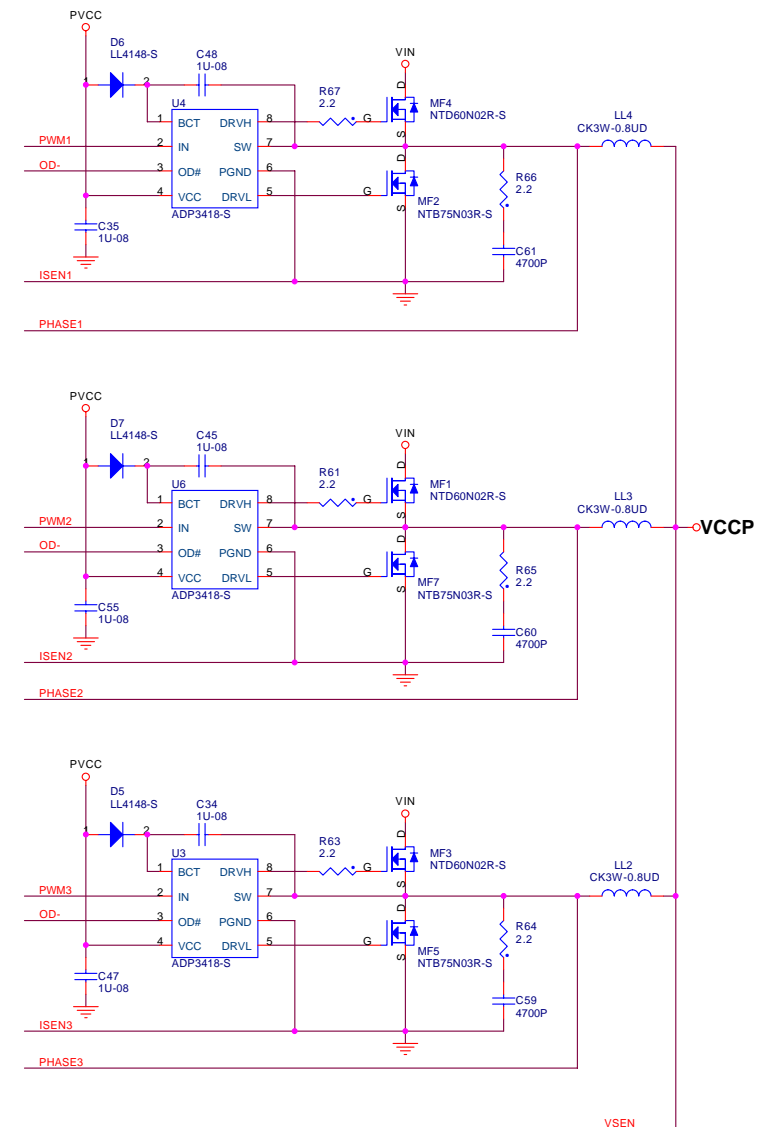
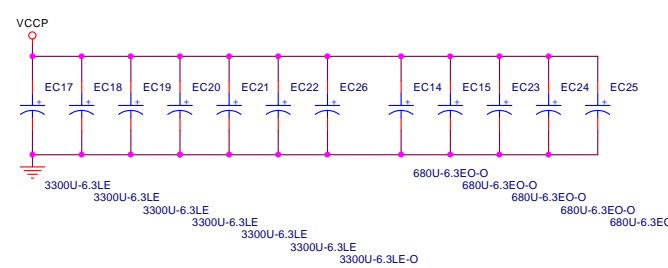
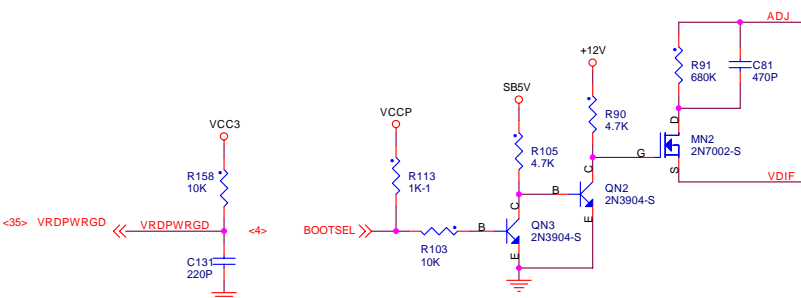
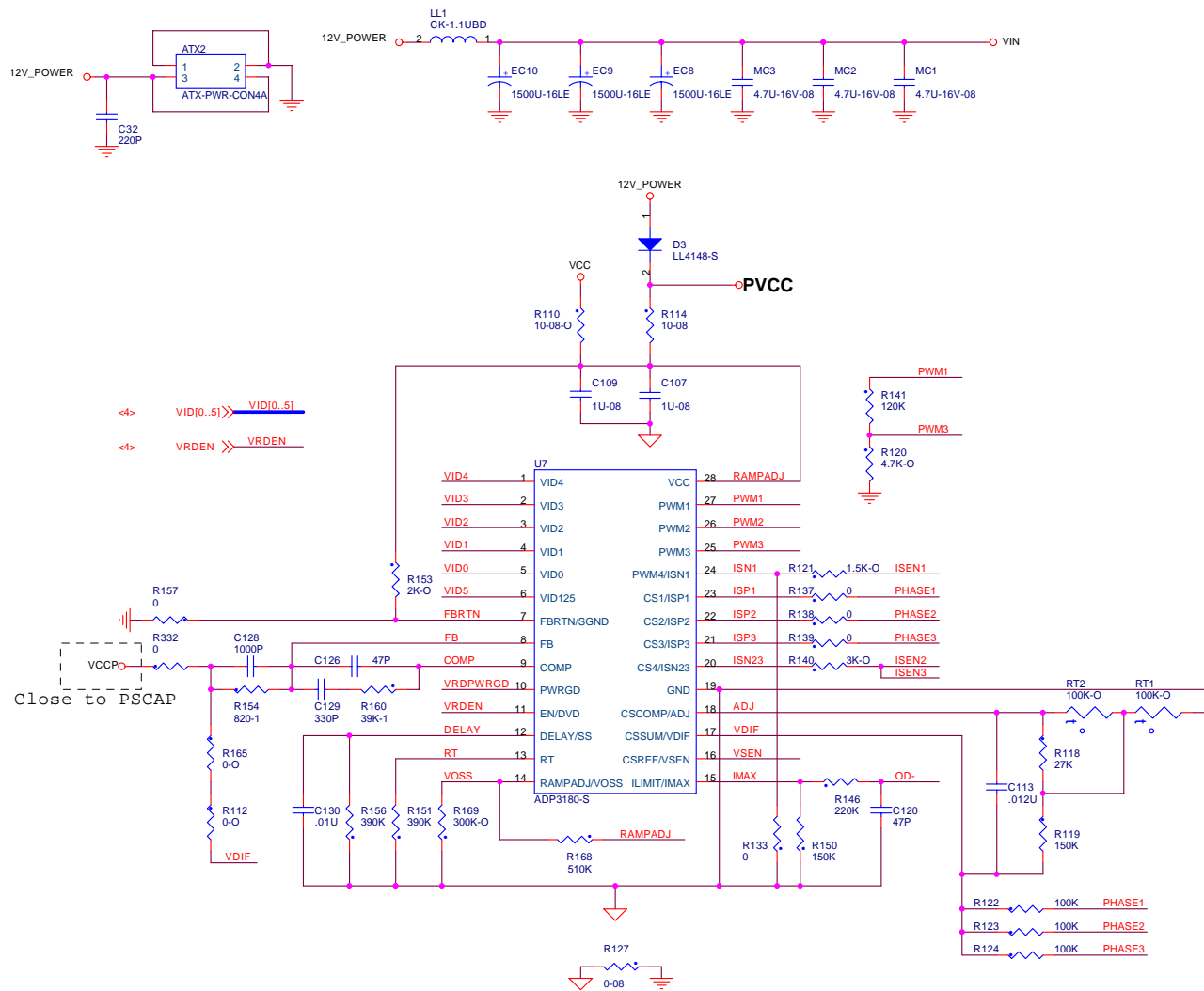
## VCC3\_DUAL

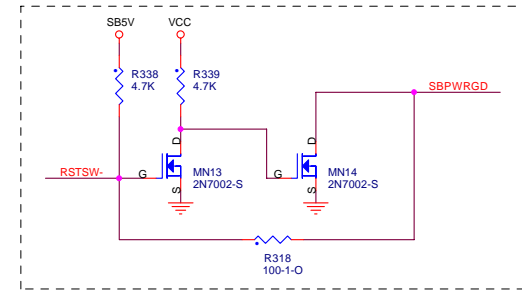
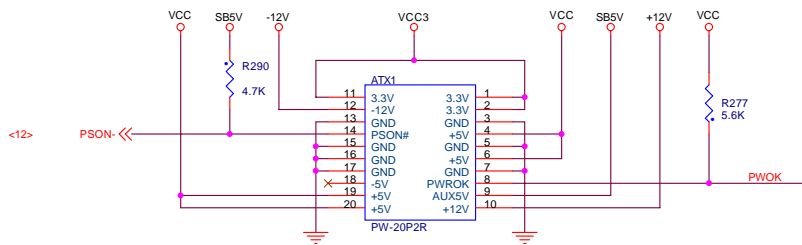
AUX\_IVDD (1.5V For NB) 10mA



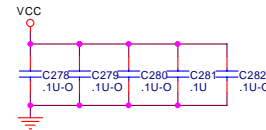
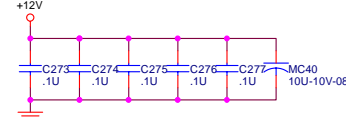
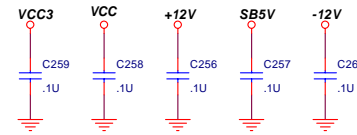
**ECS** litegroup Computer Systems

Title				<b>SF2 / 661FX</b>			
Size	Document Number					Rev	
Custom	<i>Dual 5V&amp;3V, STR</i>					1.0	
Date:	Friday, September 12, 2003	Sheet	33	of	36		

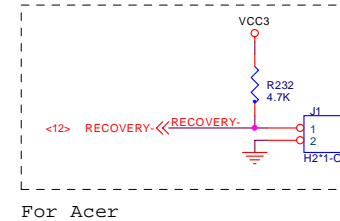
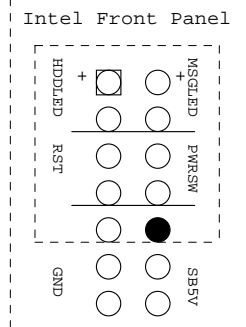




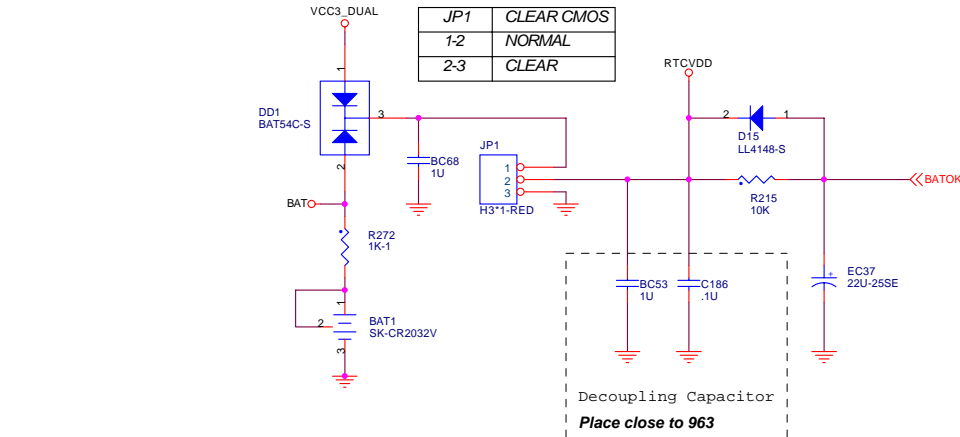
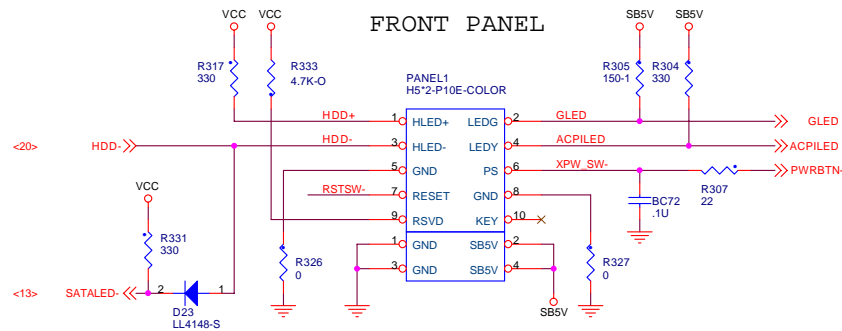
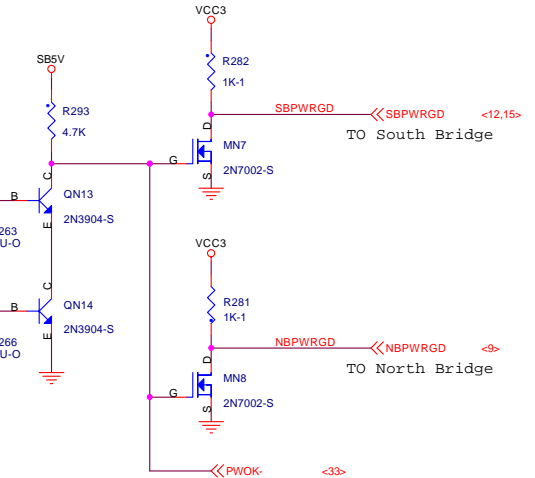
Hardware Reset Circuit



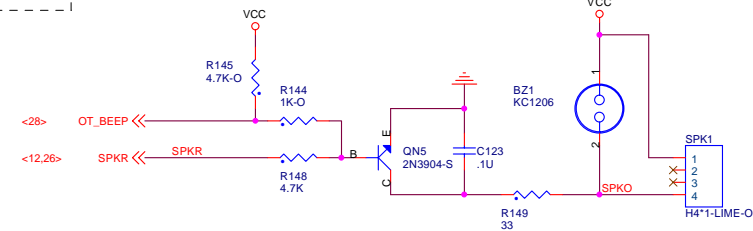
Acer Front Panel



For Acer



Decoupling Capacitor  
Place close to 963



RTC

NOTE!

- 1.The RTCVDD is 3V
  - 2.Decoupling capacitor must be close to 635 RTCVDD pin.
  - 3.RTC circuit must strictly follow SiS's recommended design
- SiS is not responsible for RTC problems from foreign designs.